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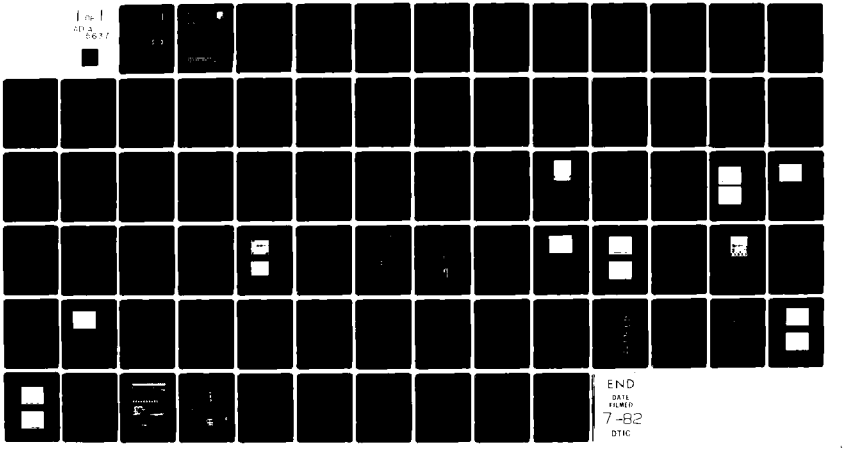

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CD APPLICATIONS STUDY

Honeywell Systems and Research Center

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Four new test structures which have been fabricated, including a first-order low-pass recursive switched-capacitor filter, a charge divider, an ED-NMOS operational amplifier, and an improved surface-channel CCD unit-delay multiplier/first-order filter, are discussed. Also included are the results of an experiment performed on the old surface-channel CCD and an ISPICE computer simulation of a switched-capacitor current-mirror half-section. An inverting switched-capacitor network is presented.

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SECTION 1

INTRODUCTION

This is the final report on Contract F19628-79-C-0176, "CCD Applications Study," and is submitted in partial fulfillment of Contract Data Item 0002.

The technical goals of this program were modeling and evaluating novel filter structures using both charge coupled devices and switched capacitor techniques. Toward those ends we completed extensive modeling of CCD split-gate filters, floating-gate sensing structures, and switched-capacitor (SC) sections. In addition, we fabricated several test structures (CCD and switched-capacitor), both to verify the results of the modeling and to demonstrate novel techniques for performing CCD charge sensing, CCD gain control, SC current mirroring, and SC current splitting.

Section 2 of this report discusses modeling of split-gate filter structures.

In Section 3 the modeling is extended to include recursive filters.

Section 4 presents design, fabrication, and test results of the test structures developed during the program. Finally, Section 5 outlines major conclusions of the study and recommendations for future work.

SECTION 2

SPLIT-GATE FILTER MODELING

During the program we carried out a comprehensive analysis of split-gate filter structures. Both surface and buried-channel devices were extensively investigated. Some of the modeling work was done in collaboration with John Pennock at Southampton University, England.

SURFACE-CHANNEL DEVICES

We have made a detailed study of the floating-gate output as used in split-electrode filters, with particular attention to the inherent depletion-capacitance-induced distortion. We started the analysis with the case of a single unsplit sense gate; current and voltage sensing are distinguished and the dc transfer characteristic is used to deduce the low-frequency distortion. We then extended the analysis to the case of a split-gate structure; for voltage sensing the movement of charge perpendicular to the direction of charge propagation to equalize the surface potential under the two parts of the split gate is included. Finally, we carried the single-gate analysis over to the case of a complete filter to enable computer simulation of the entire device. The passage along the filter of signal charge packets corresponding to an input sine wave of arbitrary frequency can be simulated; the distorted output is calculated as a function of time and the harmonic content of the output extracted.

As an example of the model, Figure 1 shows the intrinsic small-signal tap-weight error that arises with voltage sensing on a split-gate structure for various capacitive loads. Changes in tap weights alter the ratio of depletion to load capacitance and thus the sensitivity to signal charge.

Figures 2a, 2b, and 2c, as a second example, show voltage sensing with different values of load capacitance for a 63-tap low-pass filter designed using the Parks-McLellan algorithm ($F_p/F_c = 0.1$, $F_s/F_c = 0.131$, and $\delta_1/\delta_2 = 1$). The gate area is 300μm x 10μm, oxide thickness = 0.11 μm, $N_A = 10^{15}$ cm^{-3}, $V_{GO}' = 5$V (effective gate bias $V_{GO} - V_{FB}$), and the maximum charge handling capability $Q_{MC} = 5$ pC.

BURIED-CHANNEL DEVICES

Analyzing a buried-channel structure is more complex than analyzing a surface-channel device, and there is no convenient normalization to enable results to be generalized to cover all possible doping profiles and signal levels. However, by taking a range of reasonable doping levels, we derived typical distortion levels and compared their performance with surface-channel devices.

We started the analysis using the case of structures with a rectangular doping profile in the channel region. Again, a single-gate output was analyzed first for both current and voltage sensing schemes. The results obtained were then compared with those for a Gaussian doping profile, and finally a complete filter was again simulated to obtain the frequency dependence of the distortion.

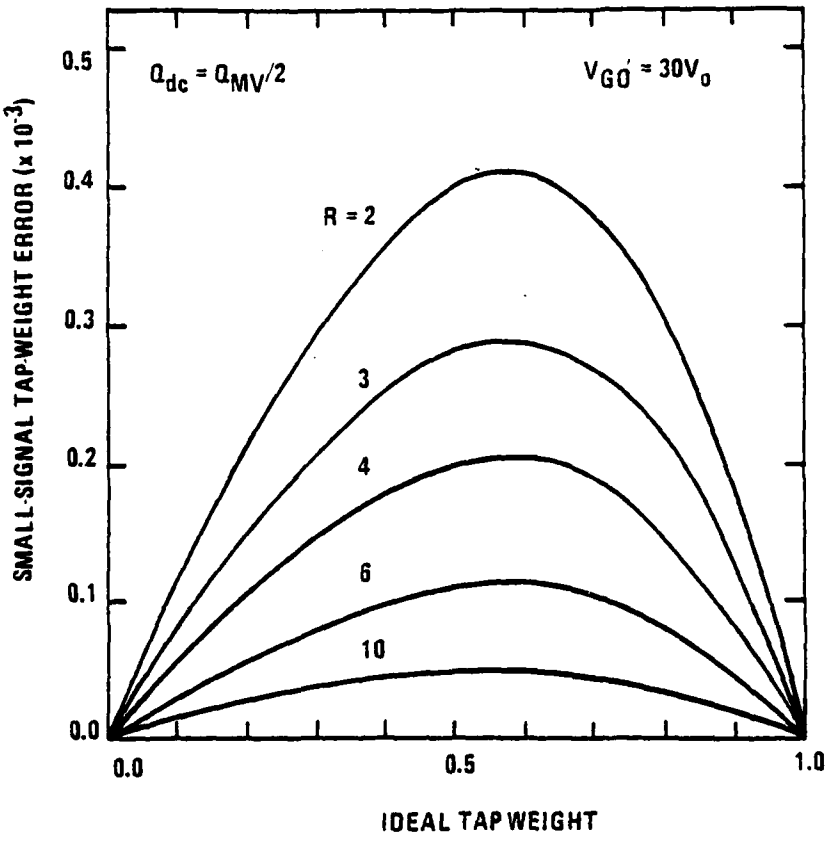


Figure 1. Single Split-Gate Voltage Sensing: Small Signal Tap-Weight Error vs Ideal Tap-Weight for Various $R = C_s/A_G C_{ox}$

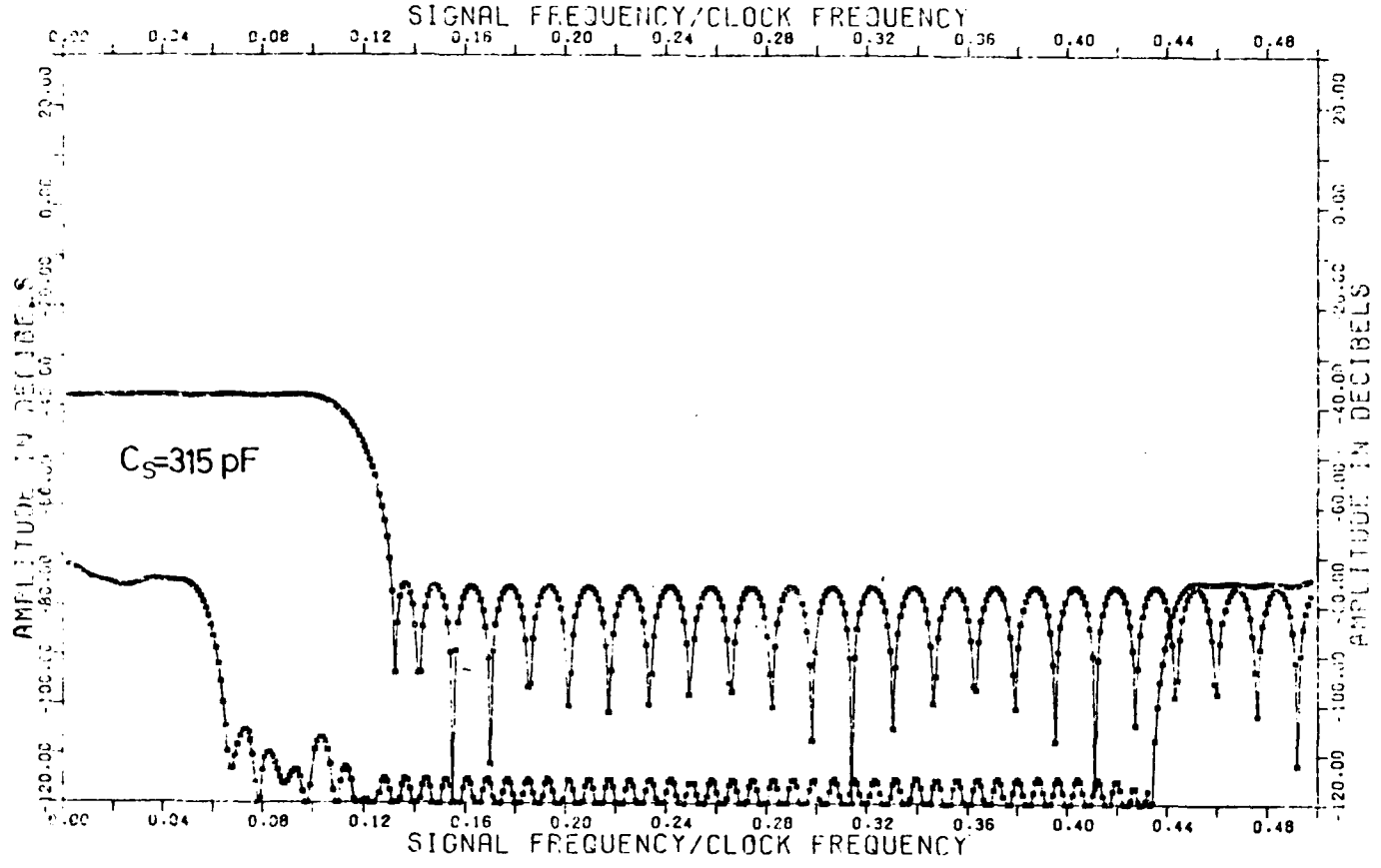


Figure 2a. Fundamental and Second Harmonic Responses of Filter: Voltage Sensing Linear Charge Input (V_{GO} = 5V, V_o = 1/6V, $Q_{pk} = Q_{MV}/4$, $Q_{dc} = Q_{MV}/2$, C_{ox} = 1 pF, 0 dB = 1V amplitude)

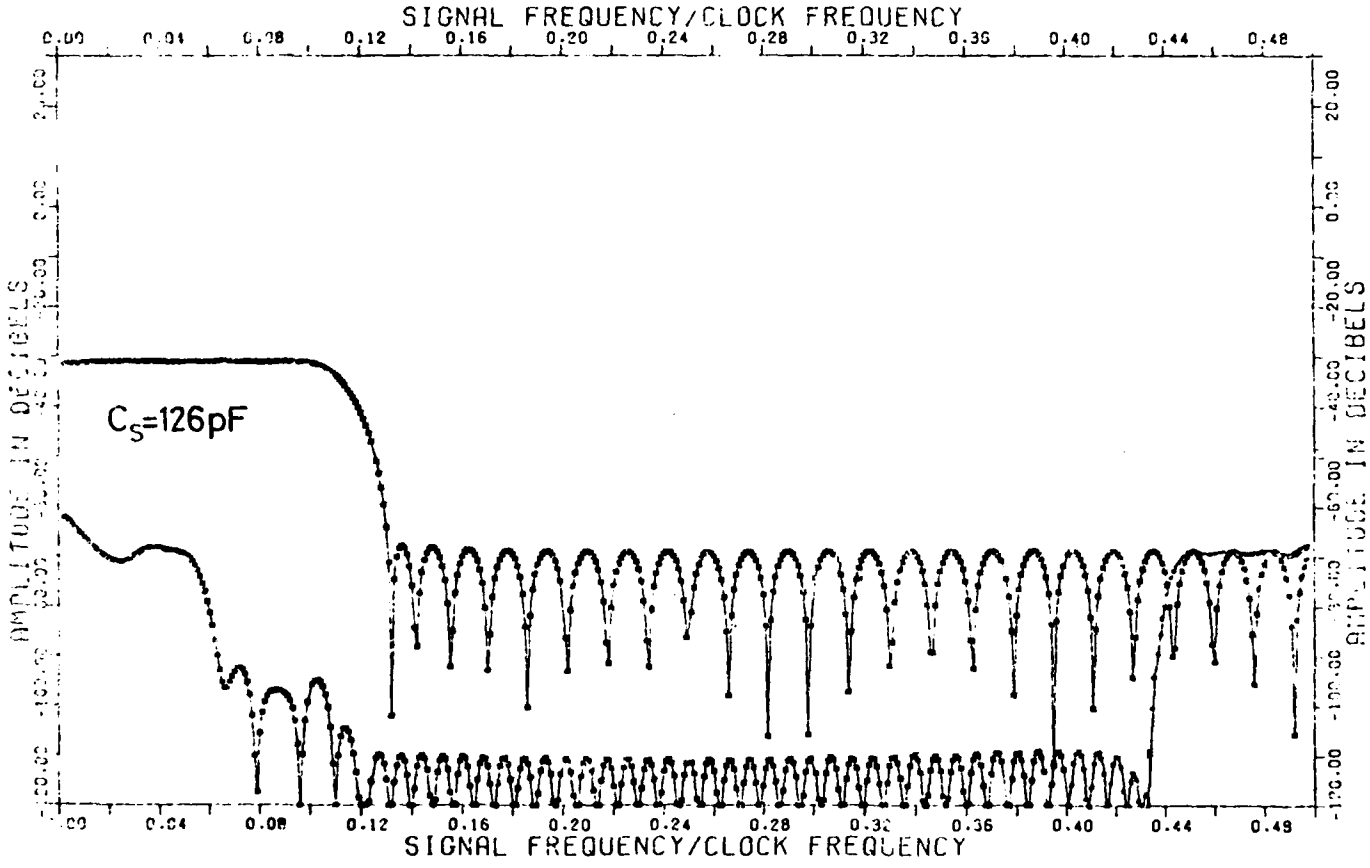


Figure 2b. Fundamental and Second Harmonic Responses of Filter: Voltage Sensing Linear Charge Input (V'_{GO} = 5V, V_o = 1/6V, $Q_{pk} = Q_{MV}/4$, $Q_{dc} = Q_{MV}/2$, C_{ox} = 1 pF, 0 dB = 1V amplitude)

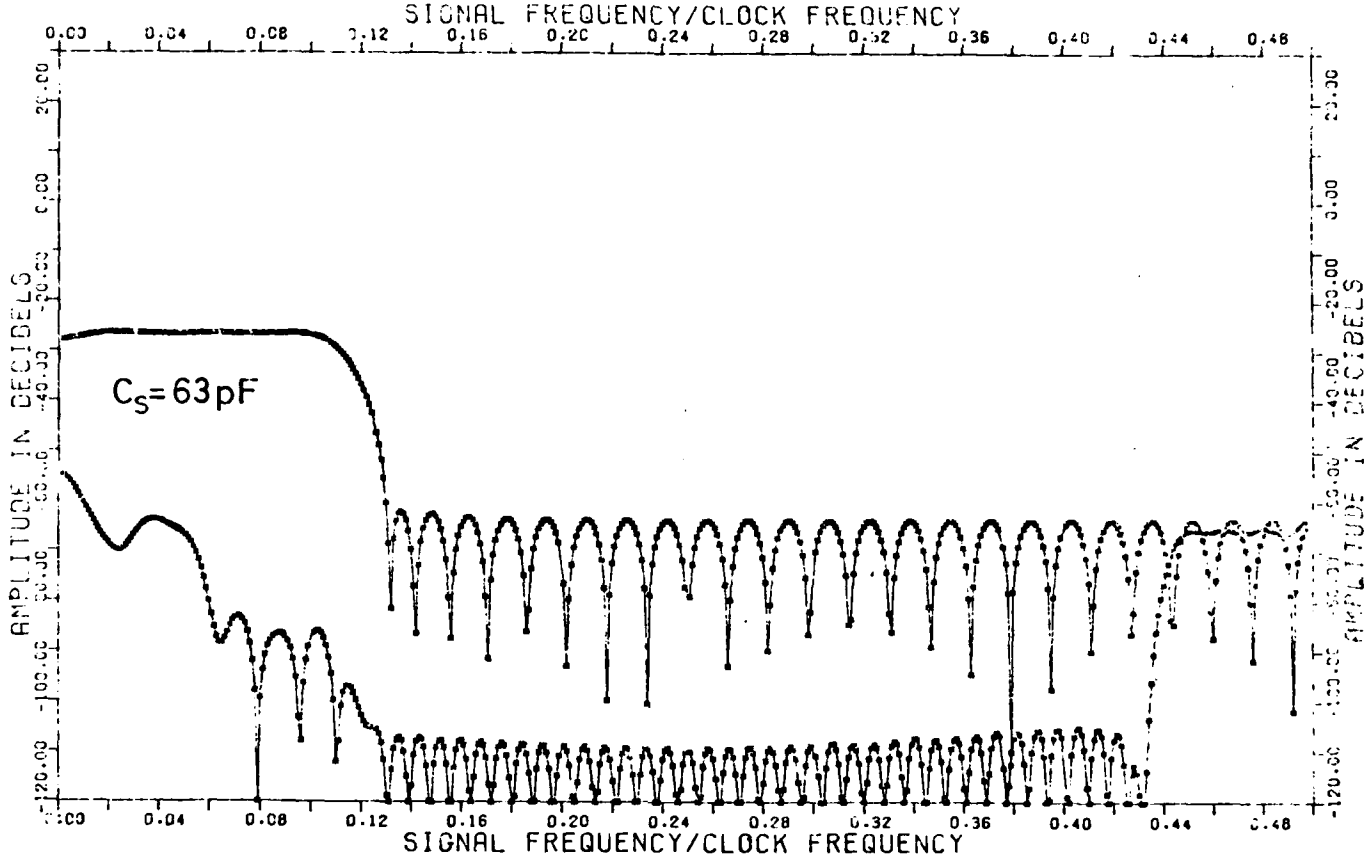


Figure 2c. Fundamental and Second Harmonic Responses of Filter: Voltage Sensing Linear Charge Input (V'_{GO} = 5V, V_o = 1/6V, $Q_{pk} = Q_{MV}/4$, $Q_{dc} = Q_{MV}/2$, C_{ox} = 1 pF, 0 dB = 1V amplitude)

An example of this analysis is demonstrated in Figure 3. This shows the harmonic distortion as a function of surface doping level in a Gaussian doping profile for voltage sensing. For the range of parameters shown, the depletion-capacitance-induced distortion for buried-channel devices is actually less than for surface-channel devices.

Figures 4, 5, and 6 show simulations of the 63-tap low-pass filter described earlier. Here we assumed a buried-channel implementation with a rectangular doping profile of $N_D = 2 \times 10^{16}$ cm^{-3}, $N_A = 10^{15}$ cm^{-3}, and oxide thickness of 0.11μm. As can be seen, the general level of distortion is very similar to that in a surface-channel device.

TRANSFER INEFFICIENCY EFFECTS

In a CCD delay line the transfer inefficiency, ϵ, attenuates high-frequency signals and causes the time delay of the CCD to become frequency dependent. In a CCD filter these effects are compounded by the dependence of the filter output on signal charges at all stages along the CCD; that is, the transfer inefficiency modifies the effective tap weights.

If ϵ is constant, then the device is still ideally a linear system, so no harmonic distortion is introduced and only phase distortion occurs. In reality, however, ϵ is a function of the charge packet size and thus will give rise to harmonic distortion.

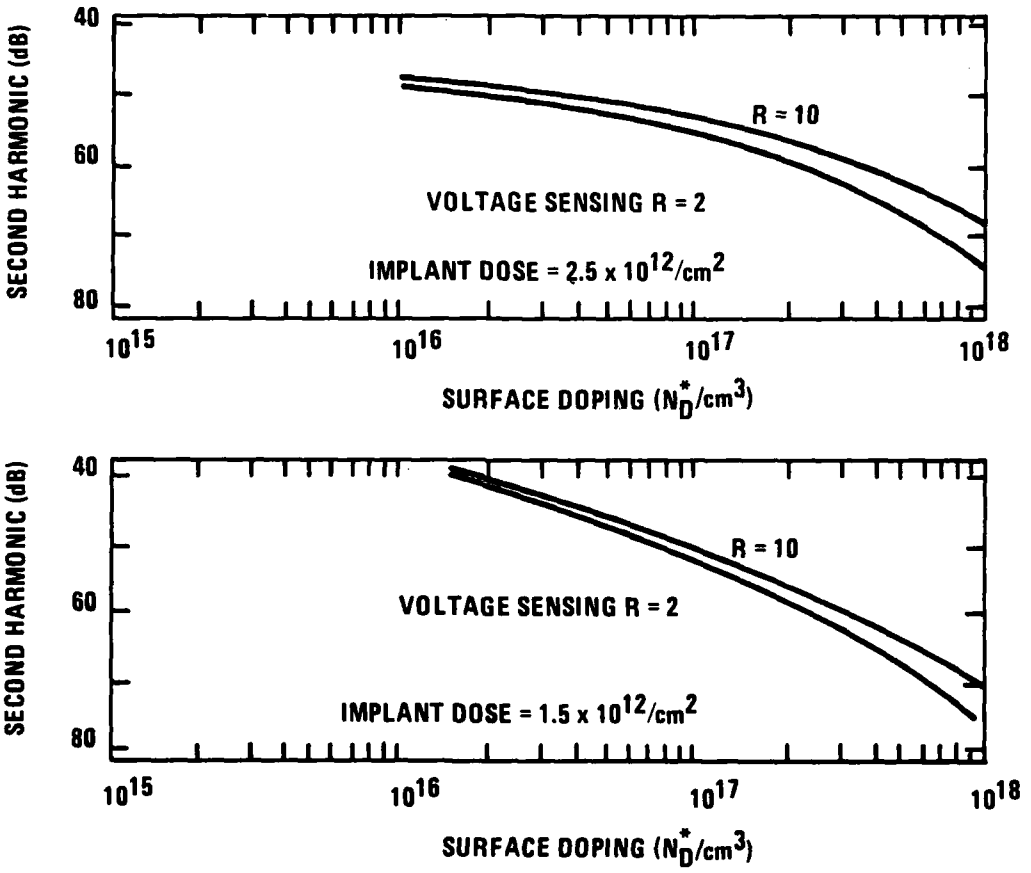


Figure 3. Harmonic Distortion (dB below fundamental) vs Surface Doping for Gaussian Doping Profile (voltage sensing) ($Q_{pk} = V'_{GO}\ C_{ox}/10$, $Q_{dc} = V'_{GO}\ C_{ox}/5$)

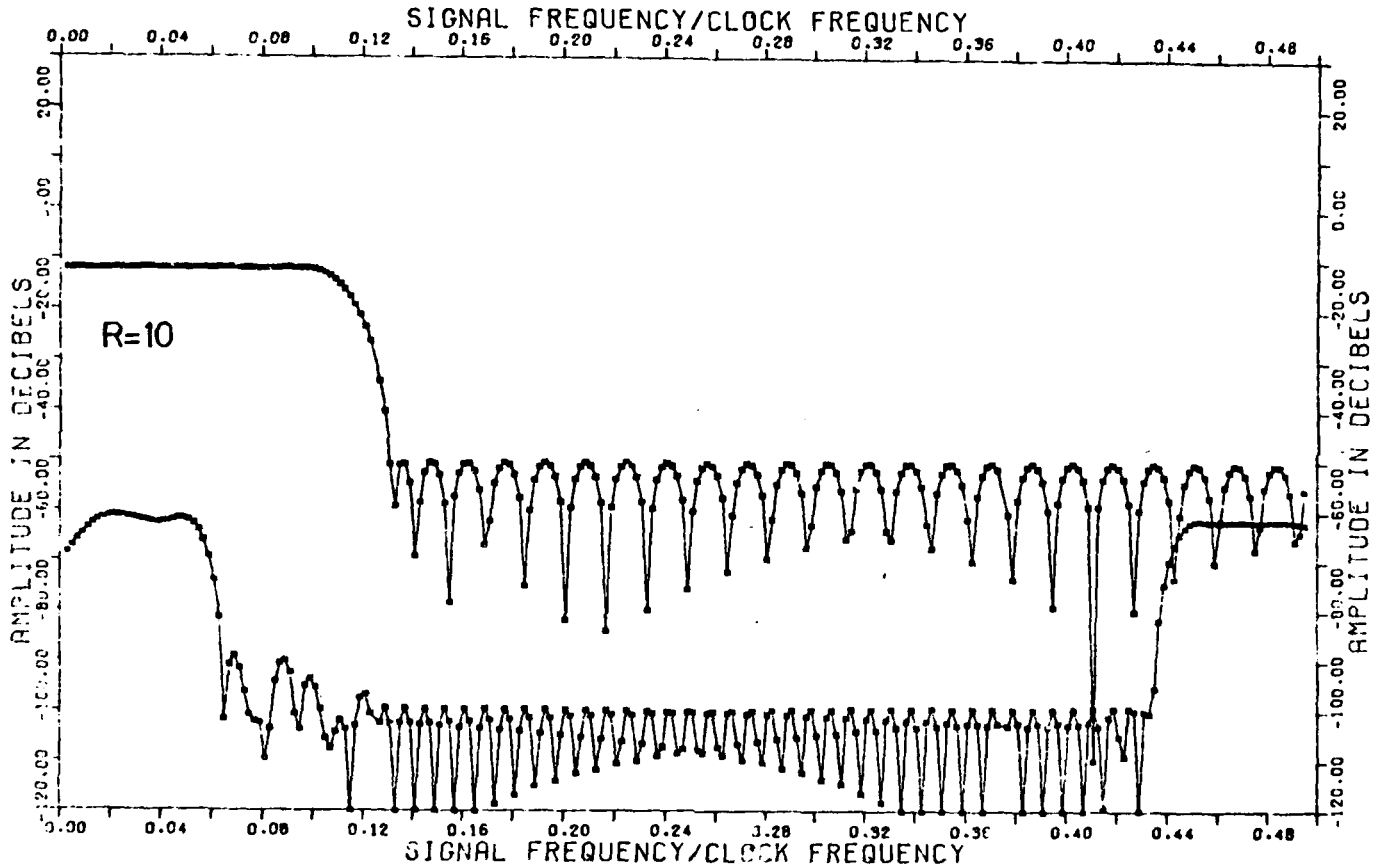


Figure 4. Fundamental and Second Harmonic for Buried-Channel Filter (N_D^* = $2 \times 10^{16}/cm^3$, $N_A = 10^{15}/cm^3$, $X_{ox} = 0.11$ μm, $X_j = 1$ μm, $V'_{GO} = 5V$, $Q_{pk} = Q_{MC}/4$, $Q_{dc} = Q_{MC}/2$)

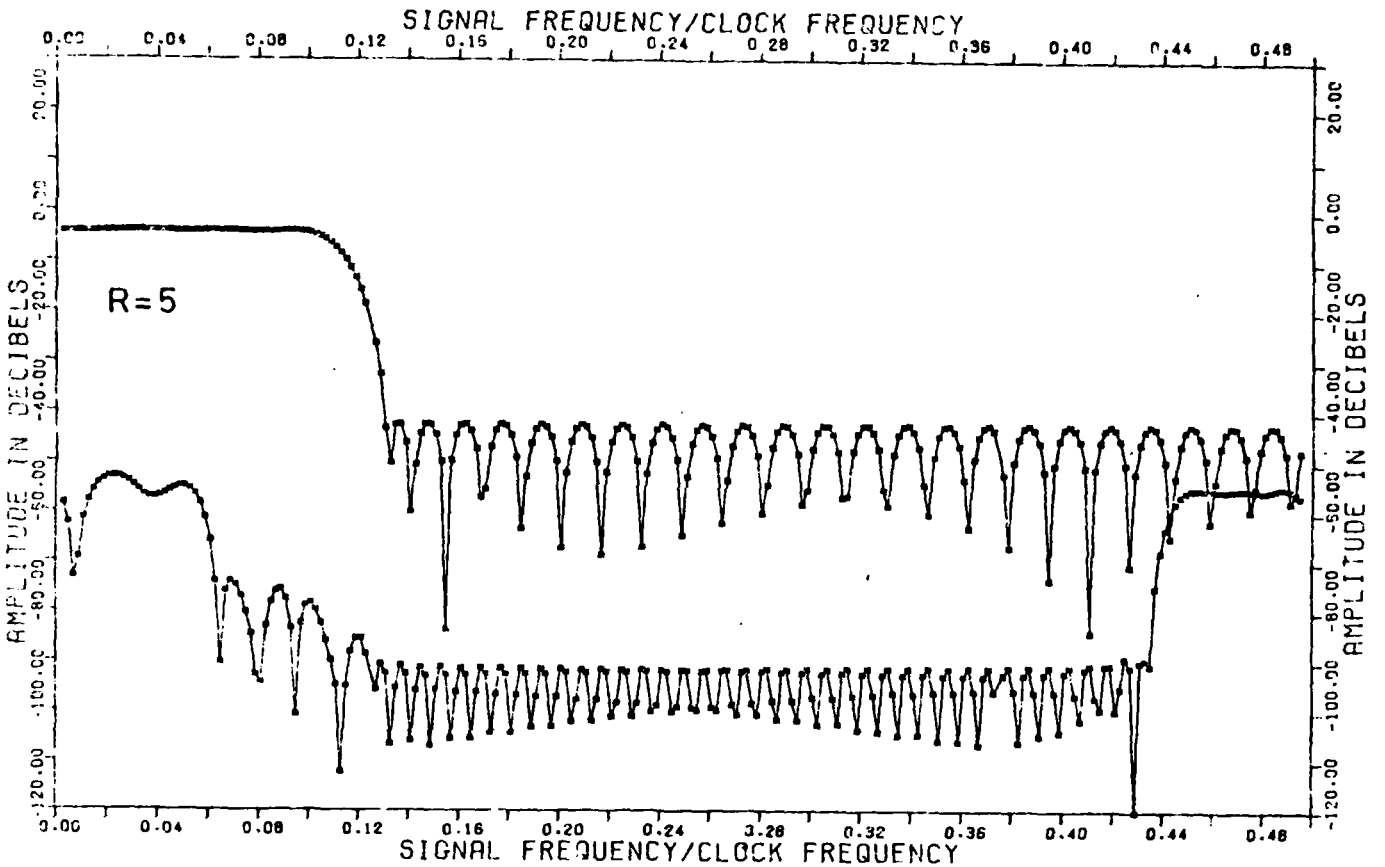


Figure 5. Fundamental and Second Harmonic for Buried-Channel Filter (N_D^* = $2 \times 10^{16}/cm^3$, $N_A = 10^{15}/cm^3$, $X_{ox} = 0.11$ μm, $X_j = 1$ μm, $V'_{GO} = 5V$, $Q_{pk} = Q_{MC}/4$, $Q_{dc} = Q_{MC}/2$)

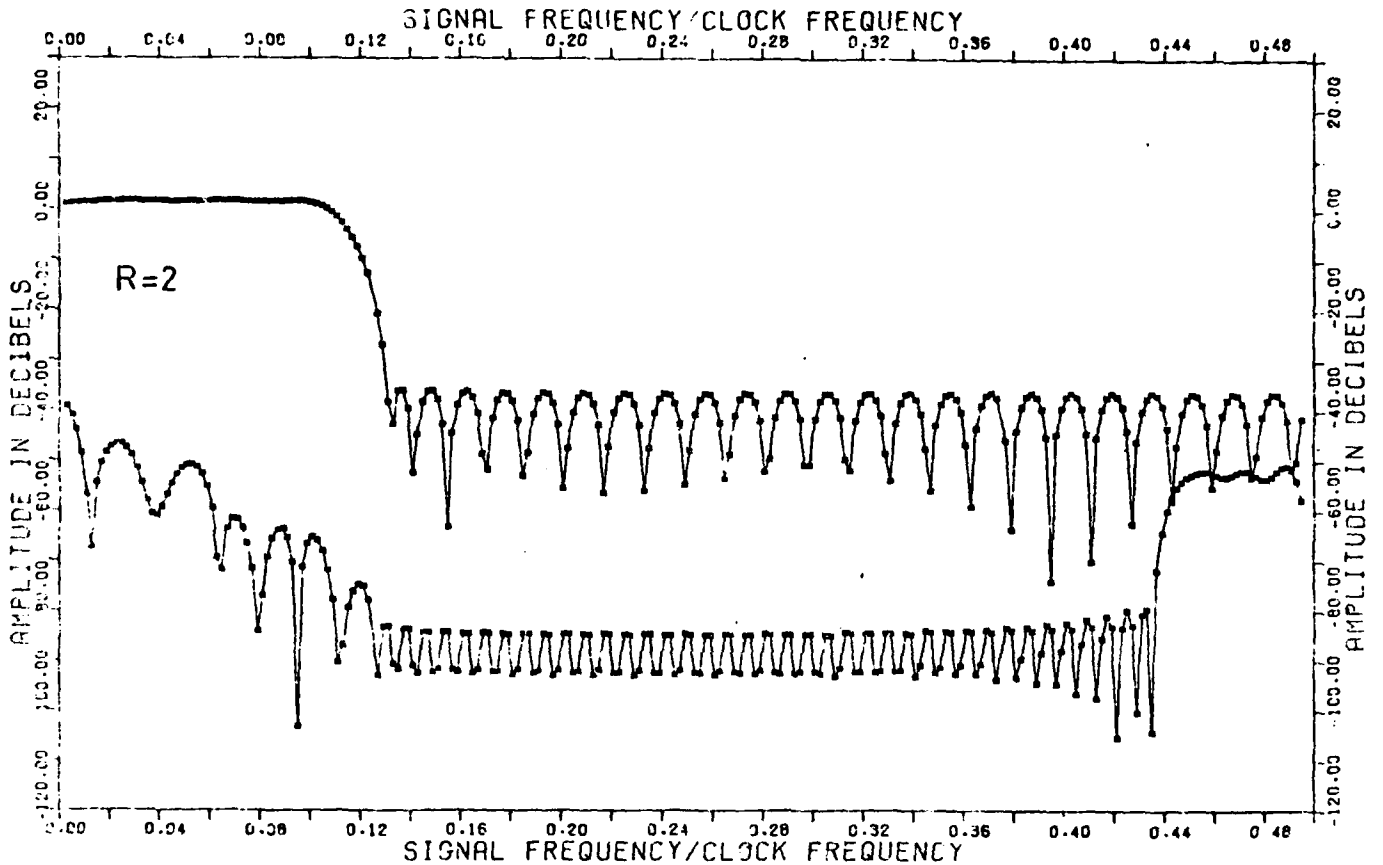


Figure 6. Fundamental and Second Harmonic for Buried-Channel Filter (N_D^* = $2 \times 10^{16}/cm^3$, $N_A = 10^{15}/cm^3$, $X_{ox} = 0.11$ μm, $X_j = 1$ μm, $V'_{GO} = 5V$ $Q_{pk} = Q_{MC}/4$, $Q_{dc} = Q_{MC}/2$)

If ϵ is not zero, a charge packet will be progressively attenuated as it passes along the device, and trailing packets will build up behind it. As the signal charge smears out, the output at any one time will be the weighted sum of several h_i, and the impulse response will be altered to $(h_i,\ i=0, \ldots, \infty)$. The impulse response is now of infinite duration, since even after many clock periods there will still be a very small fraction of the signal charge left in the device.

A modified impulse response h'_k for the filter can be derived; it is given by:

$$h'_k = \sum_{i=0}^{k} h_i \binom{k}{i} \alpha^i \epsilon^{k-i} \qquad k = 0, 1, \ldots, \infty$$

This modified impulse response implies an attenuation of the frequency response of the filter. In the passband, most of the output signal comes from the central taps, where the charge packets have undergone about N/2 transfers. An approximate model for this situation is derived by replacing the inefficient filter by the series connection of a delay line of length N/2, with transfer inefficiency ϵ and a following perfect filter. The overall frequency response will then be the sum of the ideal frequency response and the low-pass function illustrated in Figure 7.

Analysis of the effects in the stop-band is best performed via the z-transform. This shows that the effect of transfer inefficiency is to move the zeros away from the unit circle. This warping of the frequency response can be seen intuitively as follows: a nonzero transfer inefficiency delays the passage of input charge packets down the CCD, and so reduces the velocity of the input sine wave, if considered as a wave on the surface of the CCD.

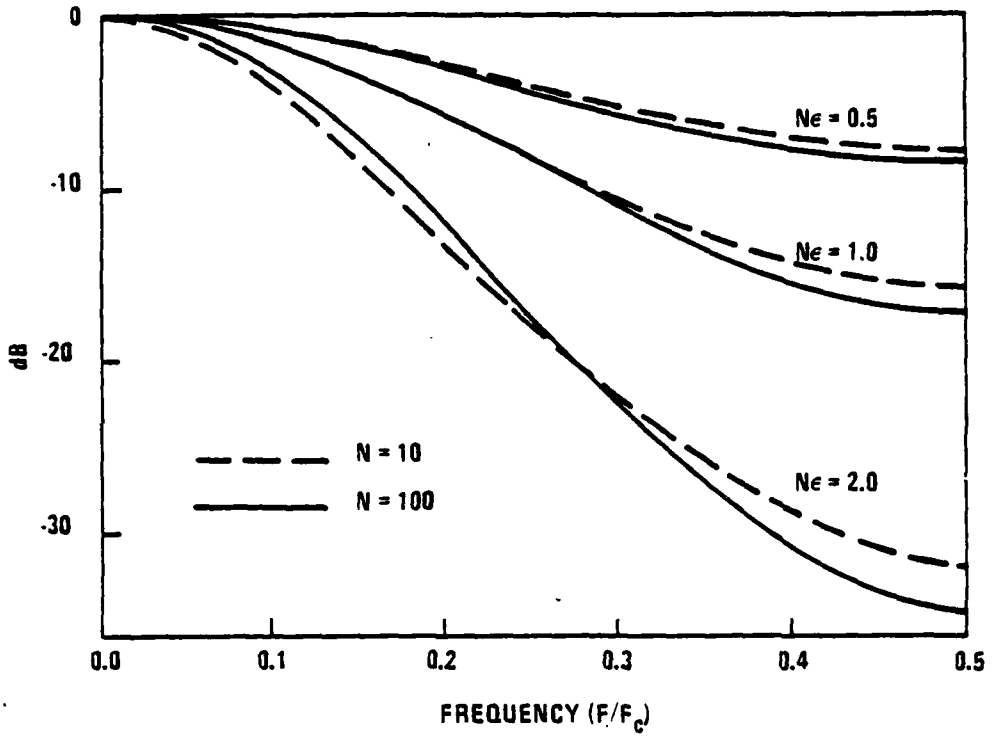


Figure 7. Frequency Response of CCD Delay Lines for Various Transfer Inefficiencies and for 10 or 100 stages

So, for a given input frequency, the wavelength will be shorter. Since the filter structure responds to wavelength rather than frequency, the filter will give an output amplitude corresponding to a higher frequency; thus the frequency response will be distorted along the frequency axis, each point being moved a distance:

$$\left(\frac{F_c}{2_\pi}\right) \varepsilon \sin\left(\frac{2\pi F_{sig}}{F_c}\right)$$

Figure 8 shows the frequency responses of the 63-tap filter for $N\varepsilon/2$ = 0.1, 0.3, and 1.0. As can be seen as $N\varepsilon$ increases, the minima in the stop-band become less sharp, the maxima are reduced, and the response tends to move towards higher frequencies. A droop in the pass-band is also apparent, as predicted by the results shown in Figure 7.

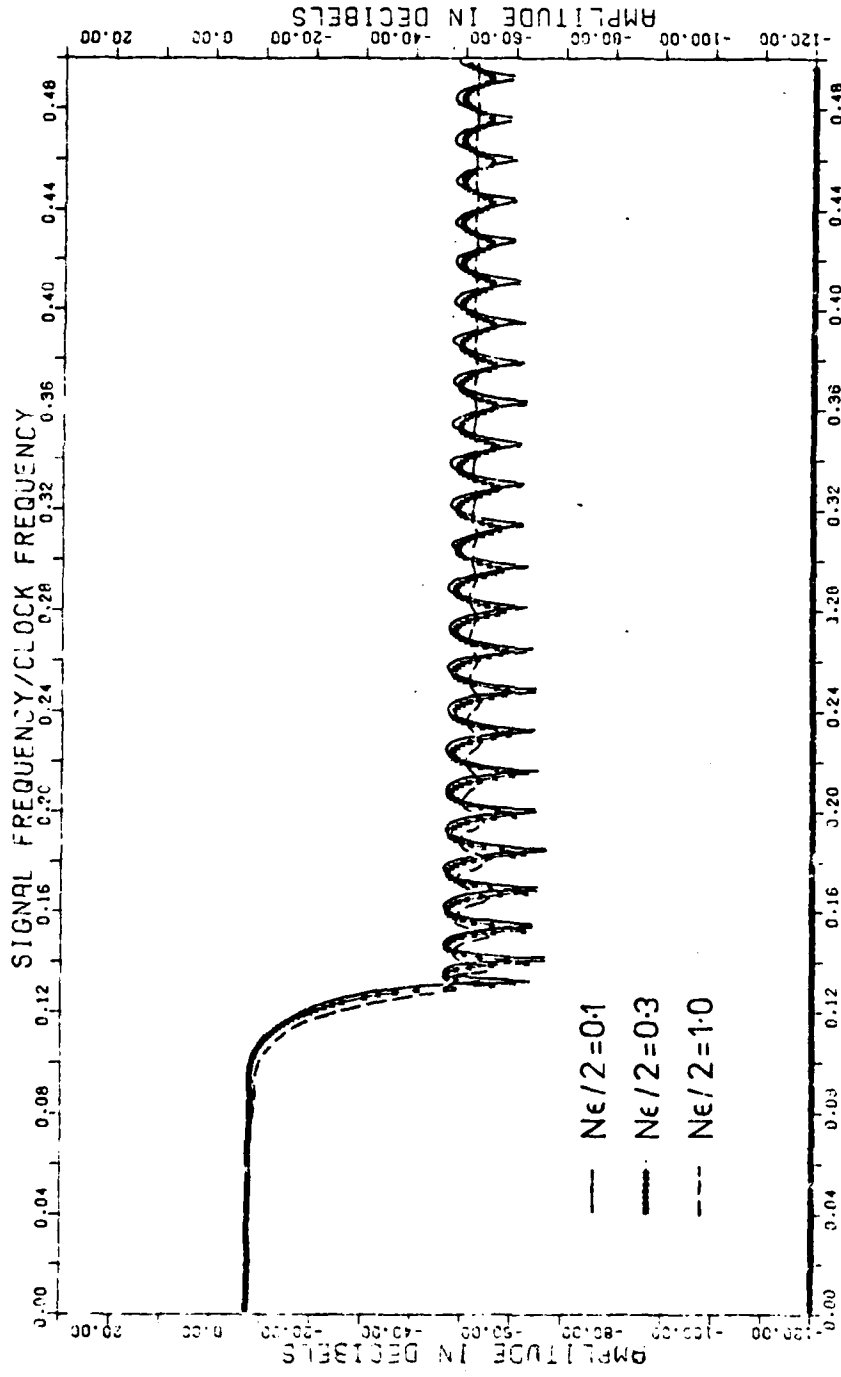


Figure 8. Degraded Frequency Responses of Filter for Various Nε

Although the average charge transfer inefficiency (CTI) is not known prior to a filter processing run, we can ask whether or not the impulse response of the filter can be pre-distorted to nullify the distortion caused by CTI. The answer to this question has been "yes" in the literature.[1] The goal is determination of a set h_j' in a p-phase device such that the total transfer function can be expressed by:

$$H(Z) = \sum_{i=o}^{k} h_i \, \lambda(Z)^i = \sum_{i=o}^{k} h_i' \left(\frac{(1-p\epsilon)\, Z^{-1}}{1-p\epsilon\, Z^{-1}}\right)^i$$

We can solve for h_i and obtain:

$$h_j' = \frac{\left\{ h_j - \sum_{i=1}^{j-1} h_{j-i}' - \binom{J-1}{i} p\epsilon^i (1 - p\epsilon)^{j-i} \right\}}{(1 - p\epsilon)^j}$$

But there are several difficulties with such an expression. First, the assumption is that all the ϵ are identical and independent of the clocking mechanism. In practice, however, ϵ is a function of signal charge packet size and is not only variable among stages, but may not even be constant among phases. In other words, if clocking of a four-phase filter, for example, is done in two-and-a-half phase fashion, the simple model may not be valid. A second major difficulty with the derivation above is that we often do not know ϵ in advance. Nevertheless, some form of compensation is desirable. Rather than attempting exact correction, however, we recommend optimizing the filter coefficients (in a least squares error sense) so that the output response is within specifications over a broad range of ϵ values. This makes a design as flexible as possible and increases device yield.

SECTION 3

DESIGN AND MODELING OF CCD AND SWITCHED-CAPACITOR (SC) RECURSIVE FILTER STRUCTURES

Analysis of more sophisticated CCD and switched-capacitor structures requires additional modeling. We have developed several routines (suitable for use on Hewlett-Packard equipment) which model generalized surface- and buried-channel CCD structures as well as switched-capacitor stages. In this section we will outline the key features of each model.

GENERAL SCCD STRUCTURES (PROGRAM FGTAP)

The analysis and design of surface-channel devices requires, at least, a solution to the one-dimensional Poisson equation with the depletion approximation. Three subroutines are needed to give a complete description of the SCCD:

1. Computation of surface potential, ψ_s, for arbitrary gate-substrate voltage with arbitrary channel charge.

2. Computation of channel charge, Q_s, for arbitrary gate-substrate voltage with arbitrary surface potential.

3. Computation of change in floating-gate voltage, ΔV_{FG}, for arbitrary initial voltage, V_G^O, with arbitrary single-channel charge injection and arbitrary capacitive loading, C_s, of the single floating gate.

We must solve three equations for the above. In an N-channel case, these are:

$$\psi_s = V_G^{1} + V_o - \left[V_o^{2} + 2V_o V_G^{1} \right]^{1/2}$$

$$Q_s = A\, C_{ox} \left\{ (\psi_s - V_G + V_{FB}) + (2V_o \psi_s)^{1/2} \right\}$$

$\Delta V_{FG} = V_G^{o} - V_G^{Q}$, the change in gate voltage

$$= \frac{-\beta + \sqrt{\beta^2 - 4\gamma}}{2}$$

where

$$\beta = 2 \left(\frac{A}{C_s} \right) \left\{ \frac{Q_s}{A} + C_{ox} \left(V_o^{2} + 2V_o \left[V_G^{0} - V_{FB} \right] \right)^{1/2} + \left(\frac{A}{C_s} \right) C_{ox}^{2} V_o \right\}$$

$$\gamma = \left(\frac{A}{C_s} \right)^2 \left\{ \left[\frac{Q_s}{A} + C_{ox} \left(V_o^{2} + 2V_o \left[V_G^{0} - V_{FB} \right] \right)^{1/2} \right]^2 - C_{ox}^{2} \left(V_o^{2} + 2V_o \left[V_G^{0} - V_{FB} + \frac{Q_s}{AC_{ox}} \right] \right) \right\}$$

and

$$V_G^{1} = V_G - V_{FB} + \frac{Q_s}{AC_{ox}}$$

$$V_o = q\, \epsilon_s \epsilon_o N_A / C_{ox}^{2}$$

Q_s = total channel charge

A = active channel-gate area

C_{ox} = oxide capacitance per unit area

C_s = total constant load capacitance

V_{FB} = flat-band voltage.

Using the first two subroutines in sequence gives a direct calculation of charge-handling capability and input voltage-to-charge sensitivity.

GENERAL BCCD STRUCTURES (PROGRAM FGBCCD)

We have also derived, for the buried-channel floating-gate sensing case, the change in floating-gate voltage following introduction of a given signal charge and the partial derivative of the voltage change with respect to the signal charge. The starting point for this analysis is a set of charge balance equations using a model like that of Figures 9a and 9b. The equations are:

$$Q_G^0 + Q_{D1}^0 = 0$$

$$Q_G^Q + Q_{D1}^Q = 0$$

$$C_S V_{FG}^Q + Q_{FG}^Q = C_S V_{FG}^0 + Q_{FG}^0$$

We can eventually obtain:

$$\Delta V = V_{FG}^Q - V_{FG}^0$$

$$= -EX_1 + EX_0^1 + (E^2G/2) - \sqrt{DE^2G + (E^3GX_0^1) + (E^4G^2/4) + E^2F}$$

where:

$$X_0 = \frac{\epsilon_{Si}(2AX_j C_{OX} + qN_D)}{C_{OX}(2A\epsilon_{Si} - qN_D)}$$

$$X_0' = \epsilon_{Si} \frac{(2A(X_j - X_m)C_{OX} + qN_D)}{C_{OX}(2A\epsilon_{Si} - qN_D)}$$

$$X_1 = X_0 - X_0^2 - \left[\frac{2\epsilon_{Si}(AX_j^2 - V_{FG}^0 + V_{FB})}{2\epsilon_{Si}A - qN_D}\right]^{1/2}$$

$$X_1' = X_0' - \left[X_0'^2 - \frac{2\epsilon_{Si}(A(X_j - X_m)^2 - V_{FG}^Q + V_{FB})}{2\epsilon_{Si}A - qN_D}\right]^{1/2}$$

$$X_m = Q_S/qN_D$$

and

$$D = V_{FG}^0 - \frac{qN_D X_1 A_{FG}}{C_S}$$

$$E = \frac{qN_D A_{FG}}{C_S}$$

A_{FG} area of floating gate

$$F = X_0'^2 - \frac{2\epsilon_{Si}\,(A\,(X_j - X_m)^2 + V_{FB}}{2\epsilon_{Si}A - qN_D}$$

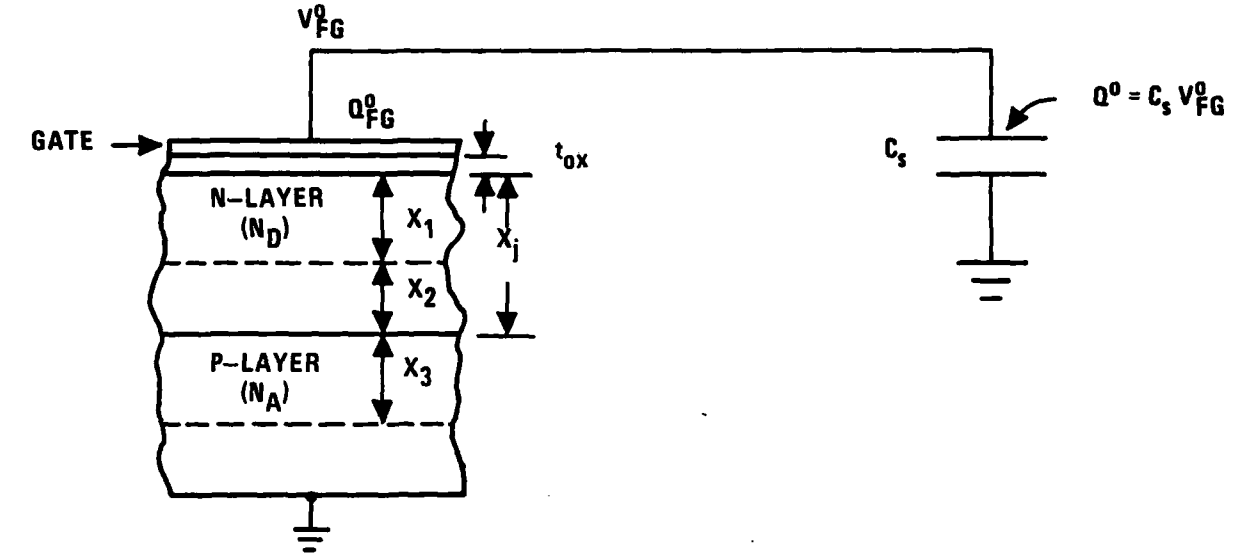
$$G = \frac{2\epsilon_{Si}}{2\epsilon_{Si}A - qN_D}$$

SWITCHED CAPACITOR CURRENT MIRROR

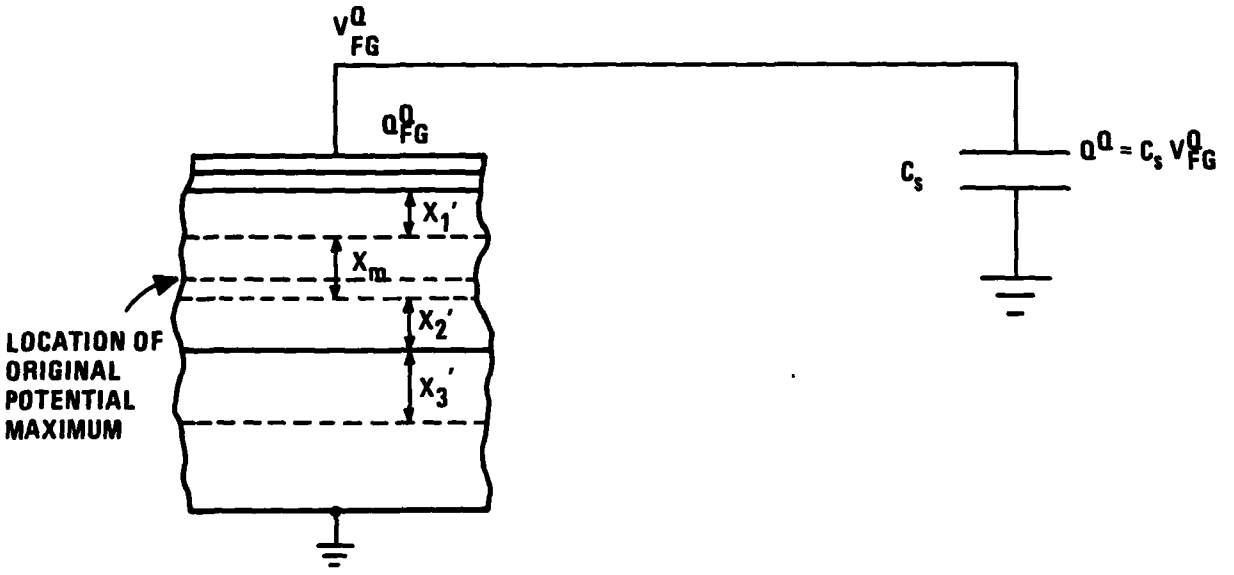
The switched capacitor realization of the multiply-delay-sum function so crucial to filter design is shown in Figure 10a. This is the Z domain equivalent of the circuit shown in Figure 10b.

The main objective of this structure is to produce a transfer function of band-pass type without the use of an operational amplifier. Charge gain is obtained by discharging an input capacitor (or capacitors) through a MOST current mirror, thereby causing a controlled discharge of a different capacitor connected to the output of the current mirror.

By using two stages of current mirror with four-phase clock pulses, it is possible to cancel out the first-order offsets due to threshold voltage ($V_T \neq 0$) and pre-charge voltage ($V_{DD} \neq 0$) residuals on the capacitors.

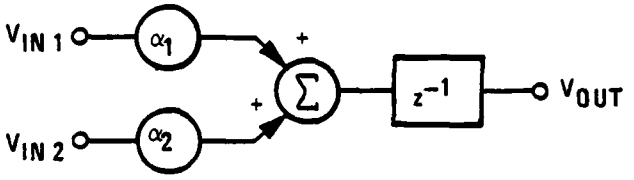


a. No charge present

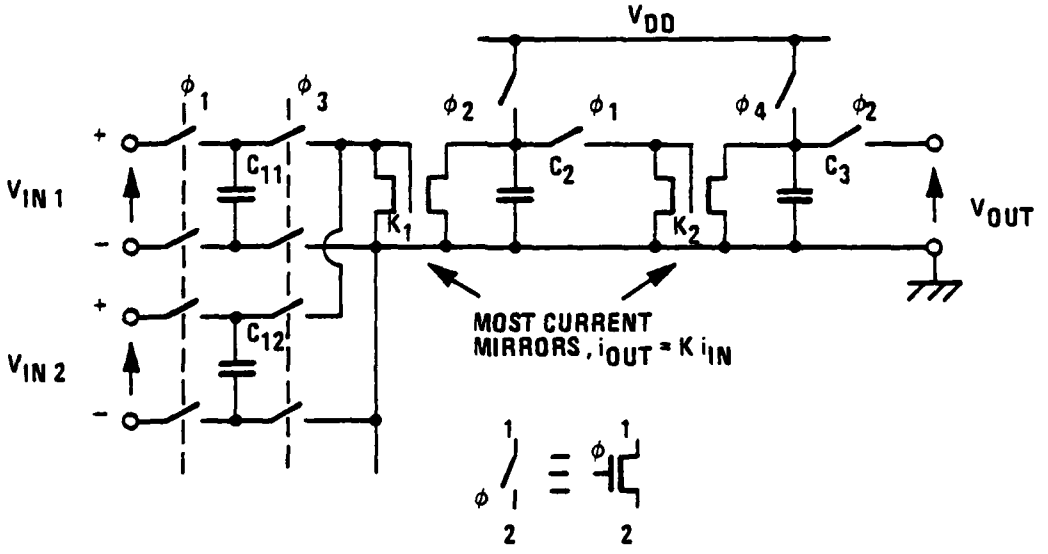


b. Channel charge present

Figure 9. BCCD Model



a. Z-domain equivalent



b. Circuit diagram of SC section. Clock phases are mutually exclusive and follow index sequence

Figure 10. Switched-Capacitor Realization of Multiply-Delay-Sum Function

The charge-domain analysis of this structure has been performed[2]; the transfer function at the beginning of phase two is given by:

$$h(Z) = V_{DD}\left(1 - K_2\frac{C_2}{C_3}\right) + V_T K_2 \frac{C_2}{C_3}\left(1 - K_1\left(\frac{C_{11} + C_{12}}{C_2}\right)\right) + \frac{K_1 K_2}{C_3}\left(C_{11} V_{IN1} + C_{12} V_{IN2}\right) Z^{-1}$$

As a result of our evaluations of the SC test structures, we deemed it appropriate to perform ISPICE computer simulations of the current-mirror half-sections. The rationale for this and the simulation results are given in Section 4 as part of the discussion of SC test chip characterization.

SUMMARY

In Sections 2 and 3 we have provided the framework for development of several test structures. In Section 4 we will outline the features of the various test structures designed and fabricated for evaluation during the program and present the test results on the structures.

SECTION 4

TEST STRUCTURE EVALUATION

As we noted earlier, the heart of any filter structure is the multiply-delay-sum unit. Improvements in that unit are usually essential for improvements in filter performance. During the "CCD Applications Study" program, we designed, fabricated, and tested several different CCD and switched-capacitor test structures. In this section we will present evaluation results on the test structures.

CCD TEST STRUCTURES

The primary goal here was use of a surface-channel, floating-gate CCD technique to obtain a time-delay and multiply function. The floating-gate detector is loaded on-chip with a voltage-controlled MOS capacitance, which is also connected on-chip to the inverting input of the B channel. The novel feature in our recursive CCD filter cell is a voltage-controlled capacitive load structure which was designed to allow a programmable range of linear response on a floating gate. This allows construction of a multiply-delay-sum function. Unfortunately, a mask manufacturing error caused a shorting link in the first test structure between the capacitor and the gate of the buffer amplifier load transistor. This gate is also connected to an input pad, so the total loading of the floating gate is greatly in excess of the design goal. However, the circuit does function as originally intended--albeit with a lower overall gain.

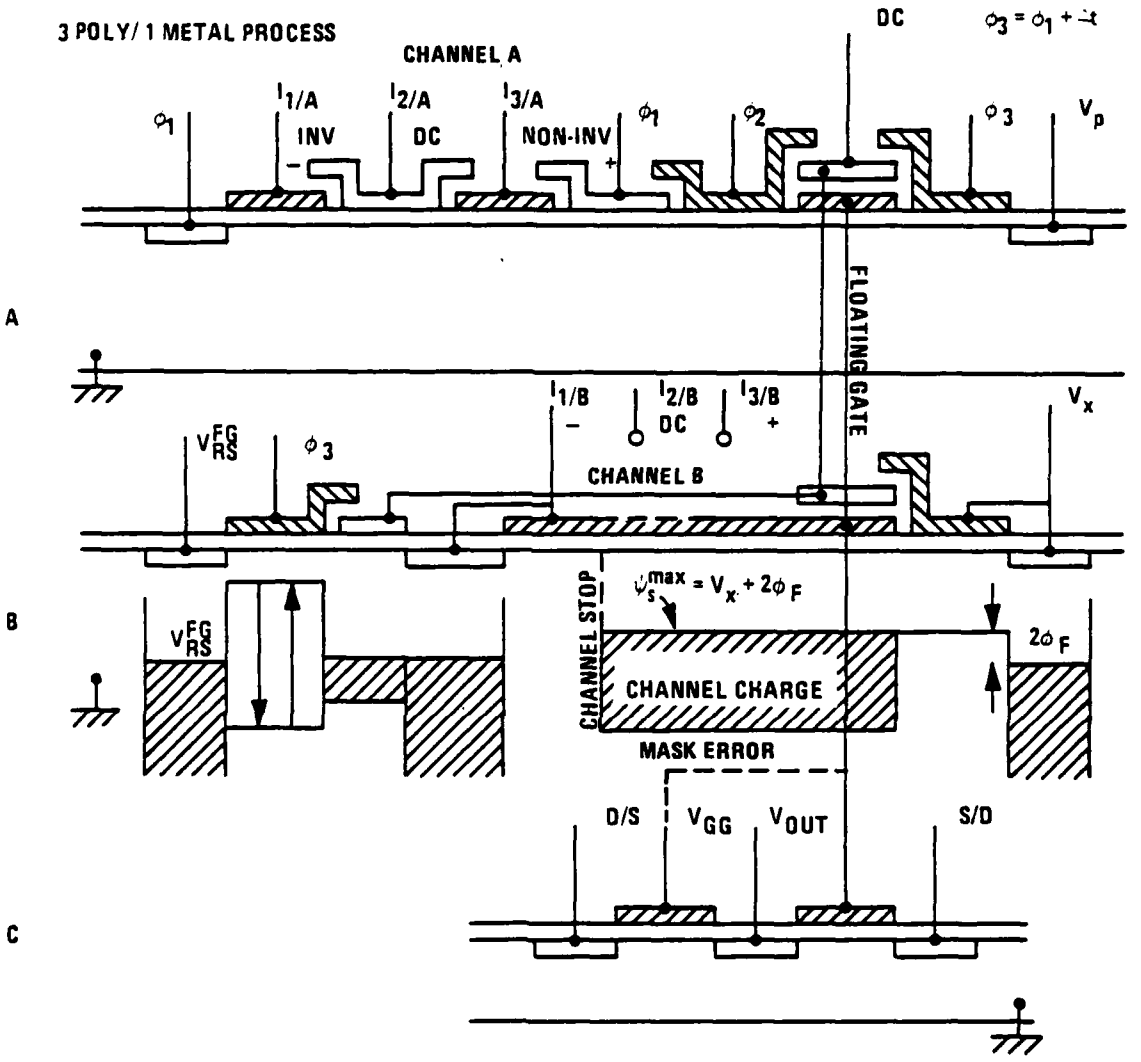
As a result of the initial characterization of this SCCD unit-delay-multiplier (UDM), several improvements were incorporated in a second test structure. The specific improvements were:

1. The multiplier capacitor has been repositioned so that the floating-gate section has a reduced channel length, thus maximizing the pulse response.
2. The channel A and B input gates have been made smaller to reduce floating-gate capacitive loading.
3. An extra input gate has been added to improve the screening of clock feedthrough.

We will describe the two test structures in separate subsections below.

SCCD UDM TEST STRUCTURE 1

A cross-section of the surface-channel test structure showing the three major components is shown in Figure 11, and a photograph of the circuit in Figure 12. The predicted behavior of the capacitive load structure with gate voltage and voltage control V_X is shown in Figure 13, while Figure 14 shows the measured characteristics. As can be seen, the overall agreement between the predicted and measured characteristics is very good, with the exception of the kinks in the deep-depletion portion of the experimental characteristic. At present, we feel that this may be a surface-state capacitance effect because the flatband voltage on these devices is larger than we expected. However, this should not cause a problem with the load element operation because a typical operating point would have V_{GG} around 10V and V_X around +2V with a ΔV_G of -1V.



A = INPUT-SUMMING DELAY UNIT $\approx 20000\ \mu m^2$

B = ELECTRICALLY-PROGRAMMABLE CAPACITANCE LOAD $\approx 4500\ \mu m^2$

C = OPTIONAL BUFFER $\approx \frac{1800\ \mu m^2}{26300\ \mu m^2}$

(162 x 162 μm)

Figure 11. Cross-Section of SCCD Test Structure Showing Mask Error Location

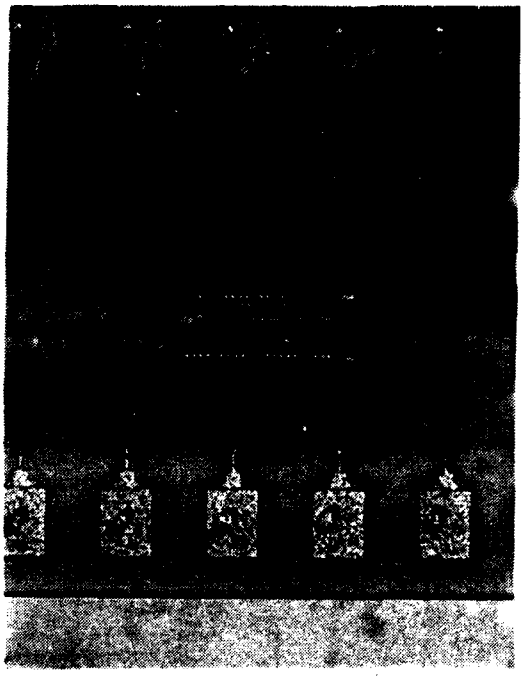


Figure 12. SCCD Test Structure (The V_x control input pad is at top right)

Figure 15 consists of three oscillograms showing the input (top trace) and inverted output (bottom trace) voltage waveforms of the unit delay multiplier under full operation of channel A. The channel B fill-spill input diode was left open during this test.

As mentioned above, V_{GG} of the buffer is short-circuited internally; no external connection is necessary.

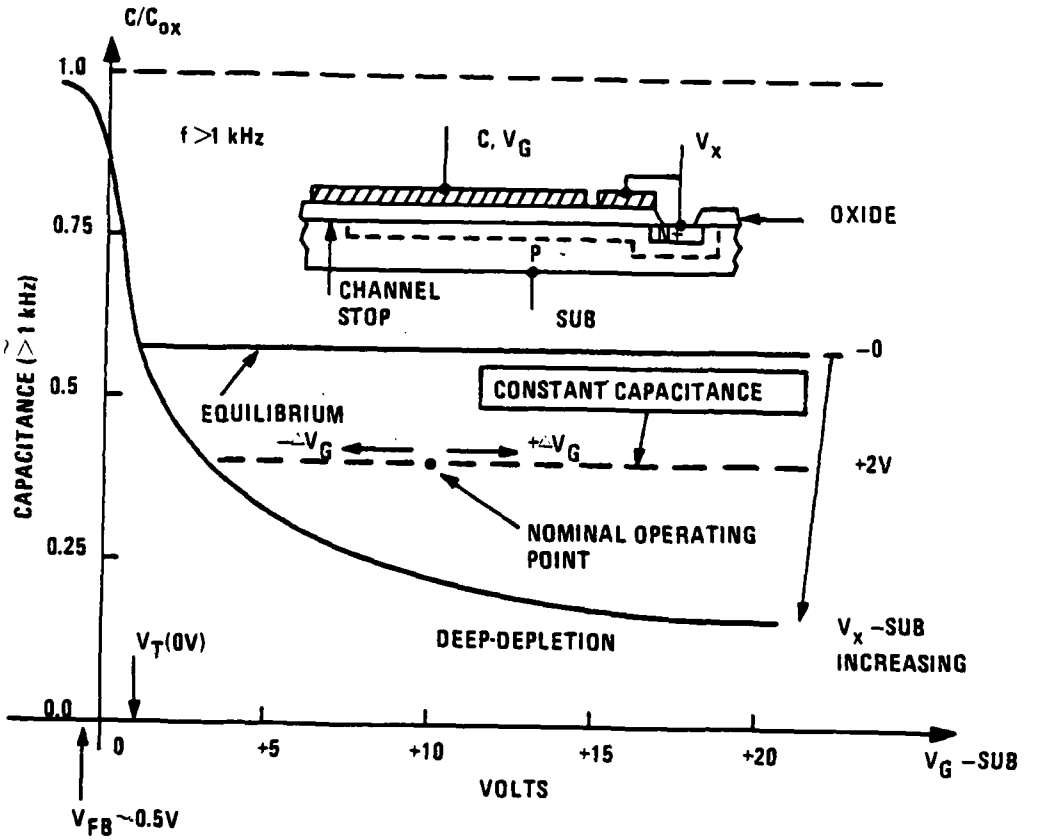


Figure 13. Expected HF Behavior ($\gtrsim$ 1 kHz) of Capacitance with Gate Voltage (V_x variation selects a new value of constant capacitance.)

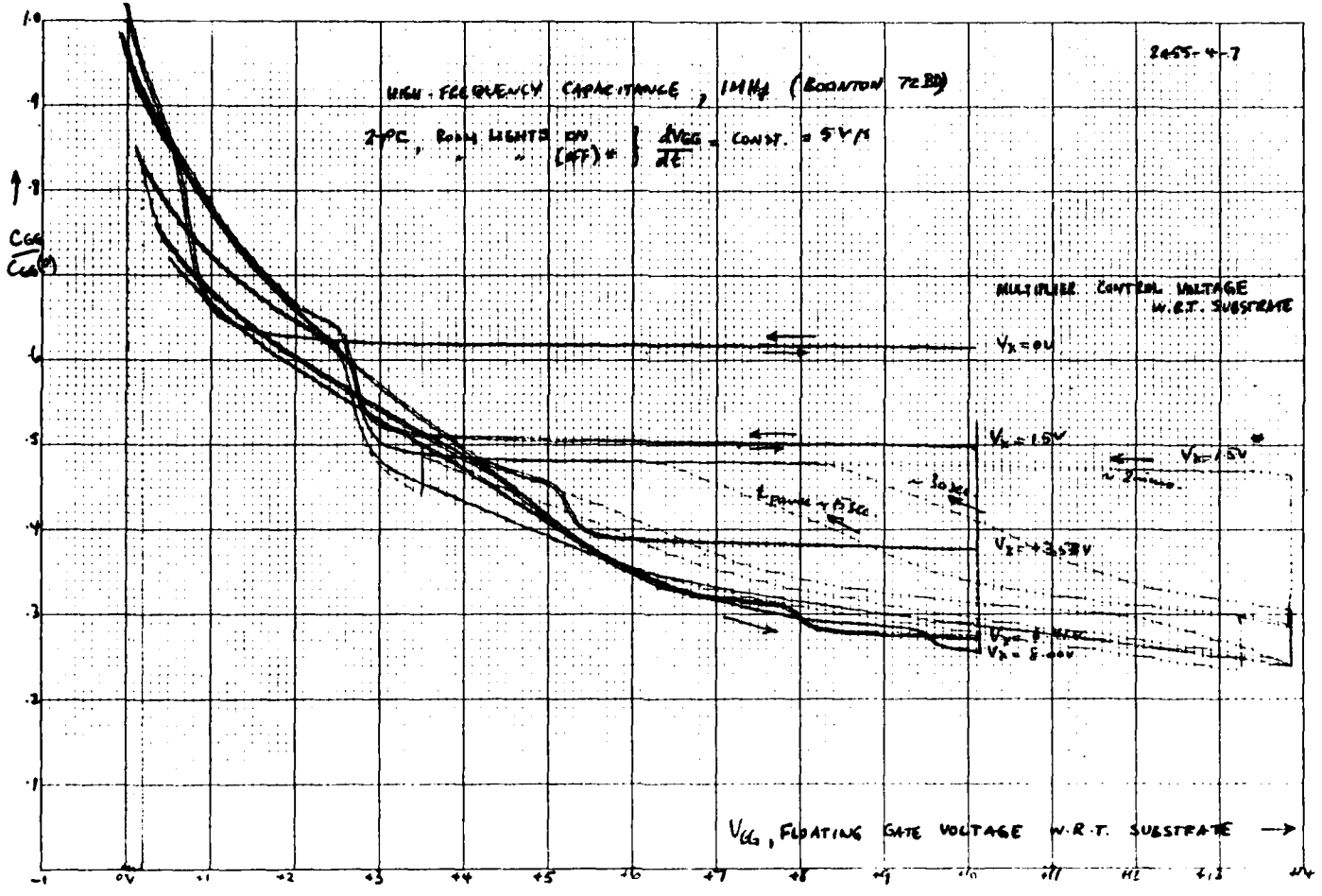
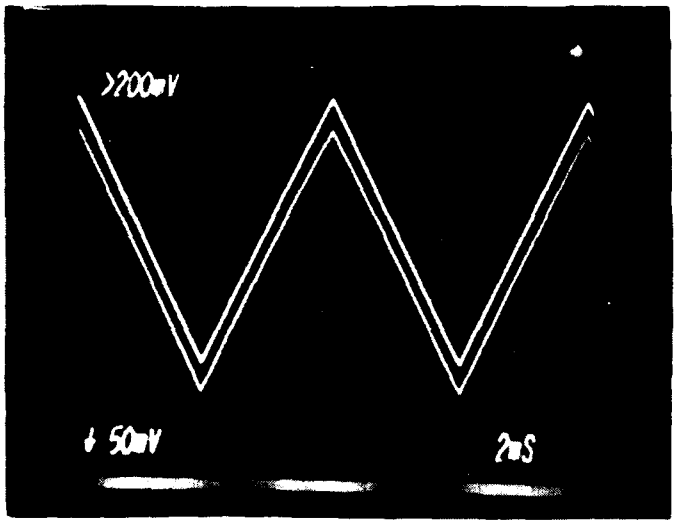
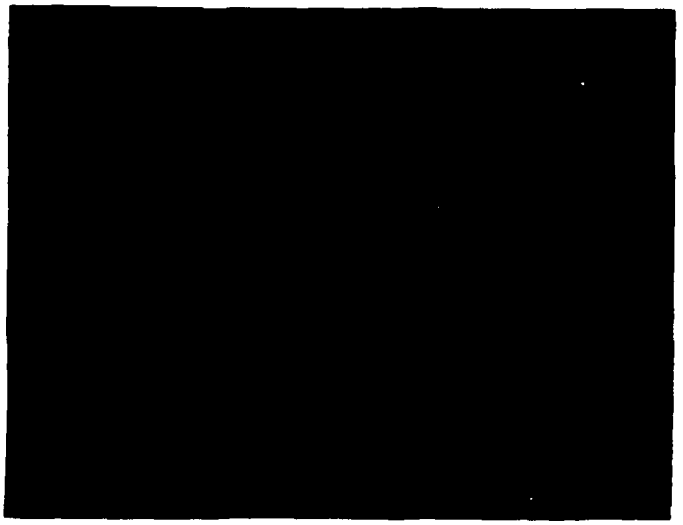


Figure 14. Measured HF Behavior of Capacitance with Gate Voltage



Oscillogram 1

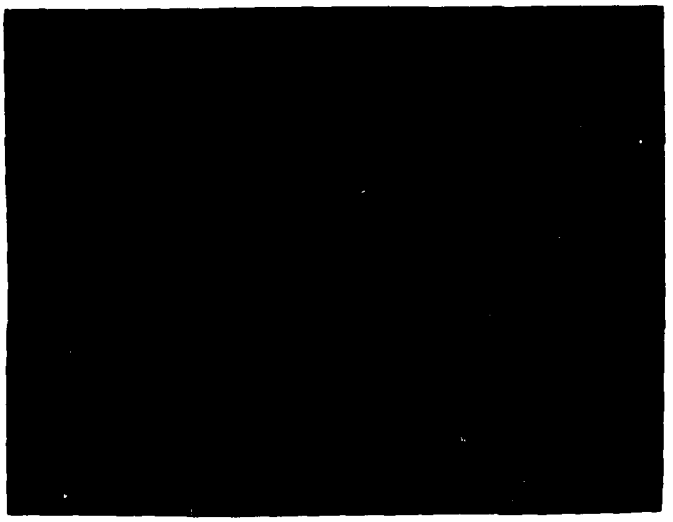
Top trace input
Lower trace output



Oscillogram 2

Zero charge being transferred to the floating gate
I_{3A} = OV

Figure 15. SCCD Characteristics



Oscillogram 3

Maximum charge being transferred to the floating gate I_{3A} = 8V

Figure 15. SCCD Characteristics (concluded)

The applied voltages are:

V_{SUB} = -3V, substrate bias

I_{3A} = input signal, 100 Hz triangle, +8.5 to +6.5V

I_{2A} = +15V, biased ON

I_{1A} = +5V, reference voltage

I_{3B} = +4V, biased ON, channel B reference voltage

I_{2B} = -3V, biased OFF

V_{SA} = ϕ_1, phase-referred input diode channel A

V_{SB} = O/C, phase-referred input diode channel B

ϕ_1 =0/15V clock, 250 kHz, 1 μsec width, 200 nsec fall time

ϕ_2 =0/15V clock, 1 μsec width, 200 nsec fall time, 100 nsec overlap ϕ_1

ϕ_3 =ϕ_1, (no reset delay in this case)

DC =+20V, screen gate

V_{RS}^{FG} =+10V, floating-gate reset voltage

V_P =ϕ_1, CCD charge sink

V_x =+10V, multiplier at minimum capacitance

S/D =D/S = +15V, load and driver used in parallel

V_{GG} =no connection

V_{OUT} =10K resistor // 10 MΩ, 12 pf scope probe

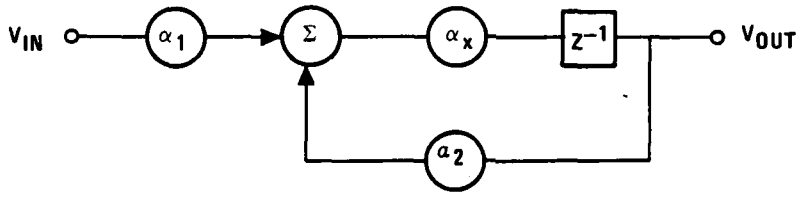
Oscillogram 1 shows the dynamic linearity. The floating gate is an inverting output with respect to charge in the channel. The buffer is operating as a conventional source follower with a resistor load of 10 kΩ.

The gain of the buffer was measured directly by using the V_{RS}^{FG} input of the reset transistor when ϕ_3 is ON 15V. The gain at DC was 0.67 when fully loaded.

The overall gain of the multiplier is evidently 250 mV/2V = 0.125. The excess capacitive loading is approximately ten times greater than intended, suggesting that the unloaded gain would be approximately unity, as required. Linearity is evidently very good. The other two oscillograms show the clock breakthrough noise plus signal. Oscillogram 2 in Figure 15

above shows I_{3A} set at OV so that no charge is transferred to the floating gate; oscillogram 3 shows I_{3A} set at 8V to give maximum charge to the floating gate. As a result of this measurement, we shielded the clock lines on our second SCCD UDM test structure to minimize their effect on the floating-gate sensing configuration.

After these preliminary tests, we operated the circuit as a recursive filter with the corresponding signal flow diagram:



$$H(z) = \frac{V_{OUT}}{V_{IN}} = \frac{\alpha_1 \alpha_x Z^{-1}}{1 - \alpha_2 \alpha_x Z^{-1}}$$

We found that clocking the V_{SB} input with ϕ_1 resulted in an extra noise spike on the output. A new clock signal for V_{SB} (ϕ_4) was generated, having a maximum value of +10V and pulsing downward to ~+8V only when ϕ_1 was in the OFF state. This eliminated the noise spike problem and confirmed that the problem was clock breakthrough to the floating gate. This was corrected in the second design, as noted above.

Exact settings for operation of the device in the recursive filter mode were noted in the second interim report. We determined the optimum circuit operation by adjusting the reference voltage to channel B and adjusting the signal range to channel A to place the output at mid-range.

The gain control function was demonstrated previously by setting V_x to a given d-c bias and observing the voltage gain of the section. There was a need, however, to measure the step response of the gain control, since this technique is being used in the regenerator of our CCD matrix processor

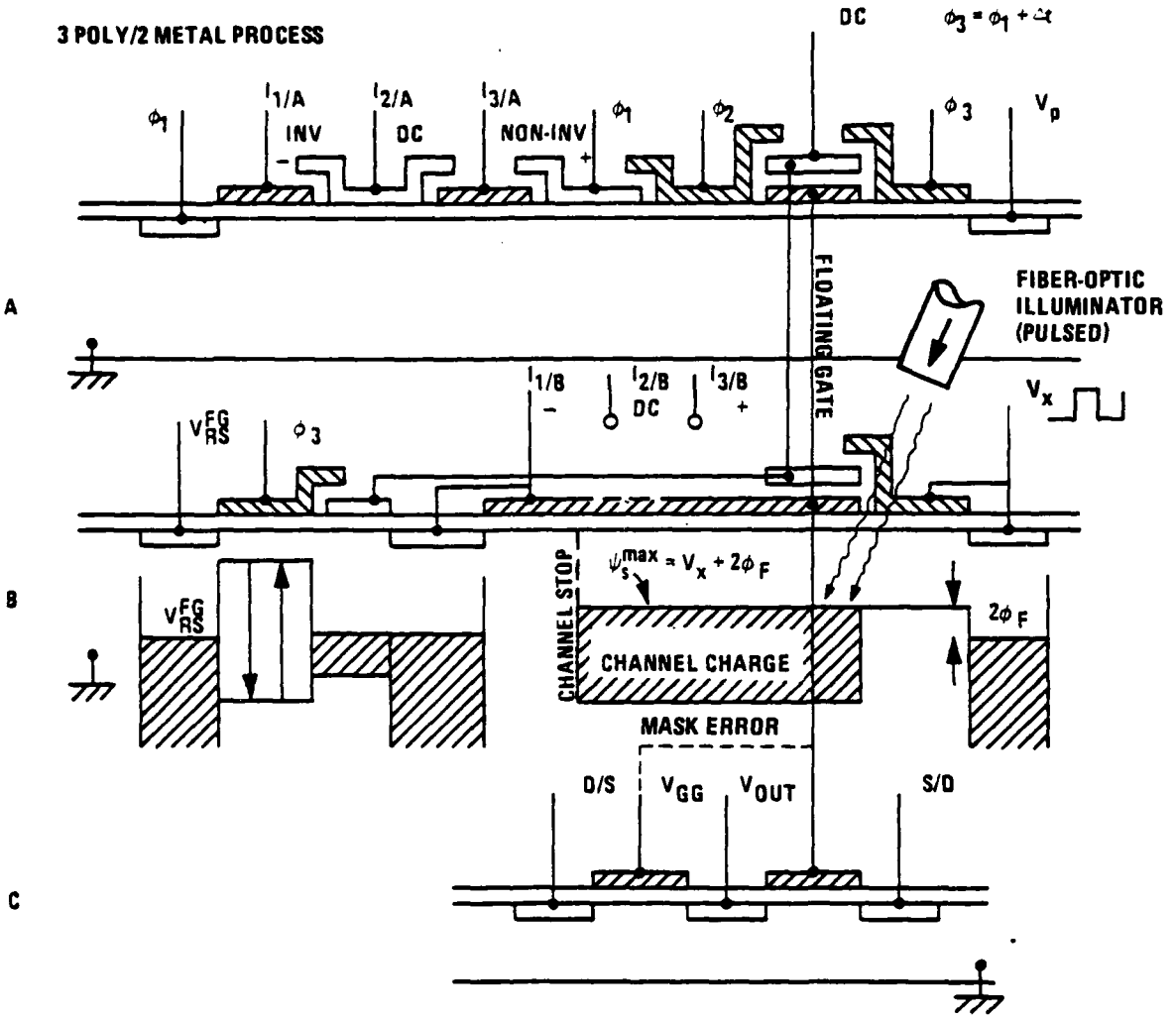
chip. In that design, the V_x gate and diode are separately accessible in order to allow fill-n-spill resetting of the channel potential under the MOS capacitor. It was necessary, therefore, to be able to reset the channel potential in the SCCD test chip without separate access to the V_x gate and diode.

An LED charge injection technique was, therefore, set up experimentally to enable localized illumination of the MOS capacitor to provide photo-generation electron-hole pairs. The electrons generated provide the channel charge needed to reset the surface potential when V_x is switched from a positive bias towards zero bias. The other direction of switching should merely spill the excess channel charge out to the diode.

The detailed test setup is described in our third interim report. We used a Spectronics GaA1As LED through a 200 μm-diameter, 54mm long fiber optic cable. Figure 16 illustrates the position of the fiber-optic cable.

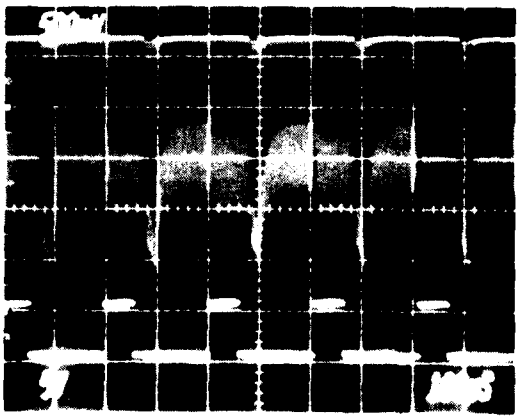
In Figure 17, oscillogram 1 shows V_{OUT} (top trace) as a function of V_x (bottom trace), illustrating clearly the change of the gain as V_x switching is followed by the illuminating LED pulse. In oscillogram 2 the heavy white line is the inverted input signal, and above it is V_{OUT}, the two triangular lines which illustrate the two gain levels.

The technique demonstrated here has very significant implications for future designs requiring parallel addressing of a matrix of gain controls. For example, the V_x gate might be driven in the cell of a matrix processor by a floating-gate detector. In that case the possibility of charge-charge multiplication would be realized on a pixel-by-pixel basis instead of globally.



A = INPUT-SUMMING DELAY UNIT	$\approx 20000\ \mu m^2$
B = ELECTRICALLY-PROGRAMMABLE CAPACITANCE LOAD	$\approx 4500\ \mu m^2$
C = OPTIONAL BUFFER	$\approx \frac{1800\ \mu m^2}{26300\ \mu m^2}$
	(162 x 162 μm)

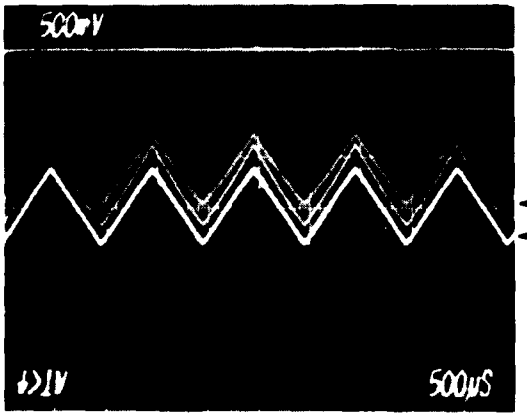
Figure 16. Cross-Section of Old SCCD Test Structure Showing LED-Fiber-Optic Cable



OSCILLOGRAM 1

V_{OUT} (TOP)

V_x (BOTTOM)



OSCILLOGRAM 2

V_{OUT} (TOP)

V_{IN} (BOTTOM

Figure 17. Oscillograms of Resetting Experiment

SCCD UDM TEST STRUCTURE 2

As mentioned above, several improvements were made in the second SCCD UDM/first-order recursive low-pass filter chip. The entire new test chip is shown in Figure 18, while the Calma layout of the SCCD-UDM structure alone is shown in Figure 19. The control node V_x, formed by the load MOS capacitor's screen gate and diode, permits infinitely variable gain adjustment of the delay section between certain limits.

Full operation of this device consisted of the connections in Figure 20. (The detailed voltage settings are outlined in Monthly Report No. 19.) The input signal was a 5-7v 1kHz triangle waveform, and the ϕ are 0/+15v 100kHz pulses.

The overall gain of the device is illustrated in Figure 21, where $\Delta V_{OUT}/\Delta I_{3A} = 0.5/1.5 = .33$. As in the previous version of this test circuit, this gain may be adjusted by changing the capacitive loading on the floating gate. As before, this is accomplished by using the V_{XG} and V_{XD} inputs to change the surface potential under the multiplier gate. The first oscillogram in Figure 22 shows the V_{OUT} of Figure 21 corresponding to a V_X of +10v; the second oscillogram shows the V_{OUT} swing reduced by reducing the V_X inputs to 0V. This change in the A.C. gain becomes less pronounced at higher input frequencies. The V_X controls would have a greater effect if the device were operated with channel B turned off--that is, as a unit-delay multiplier rather than a recursive filter.

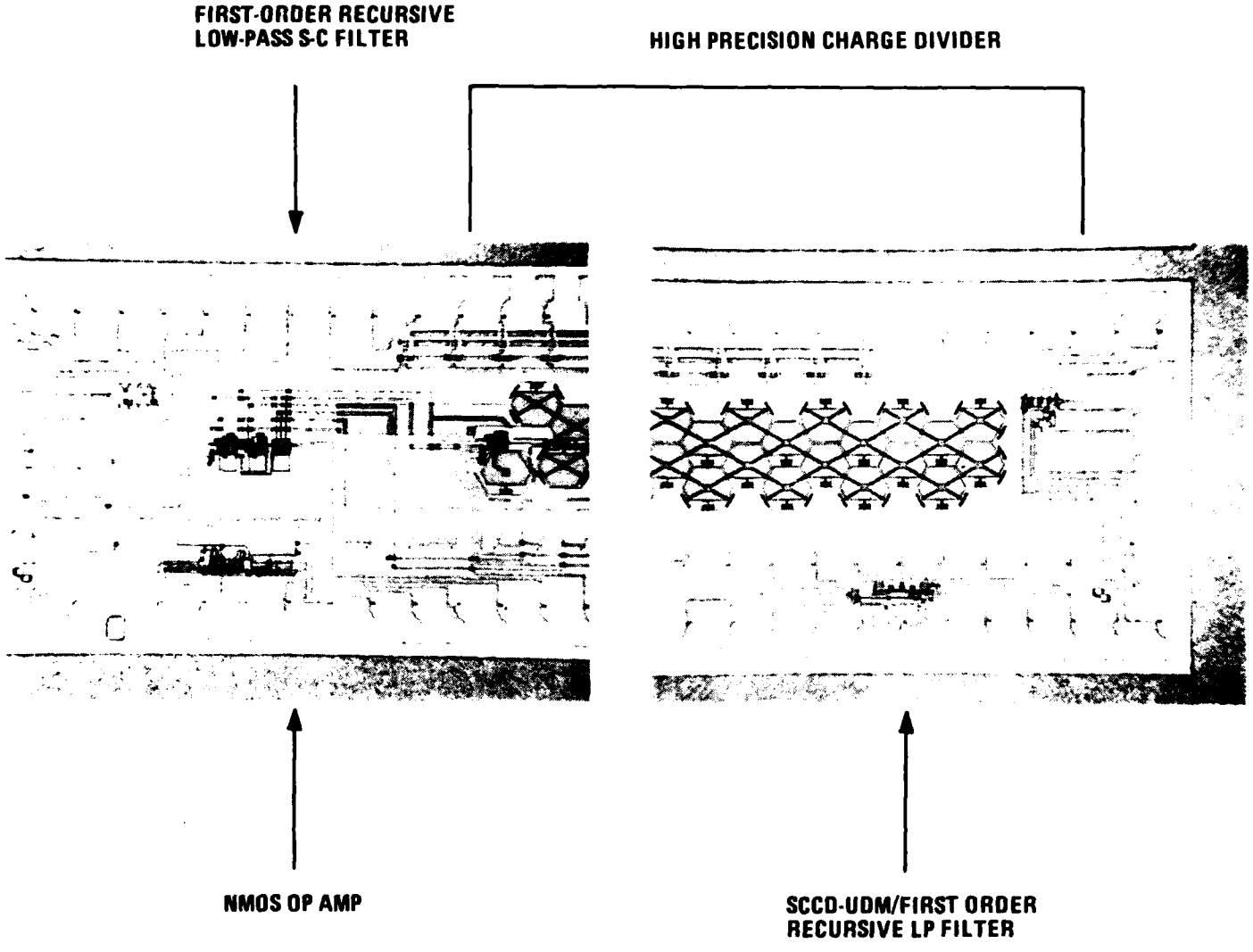


Figure 18. New Test Chip

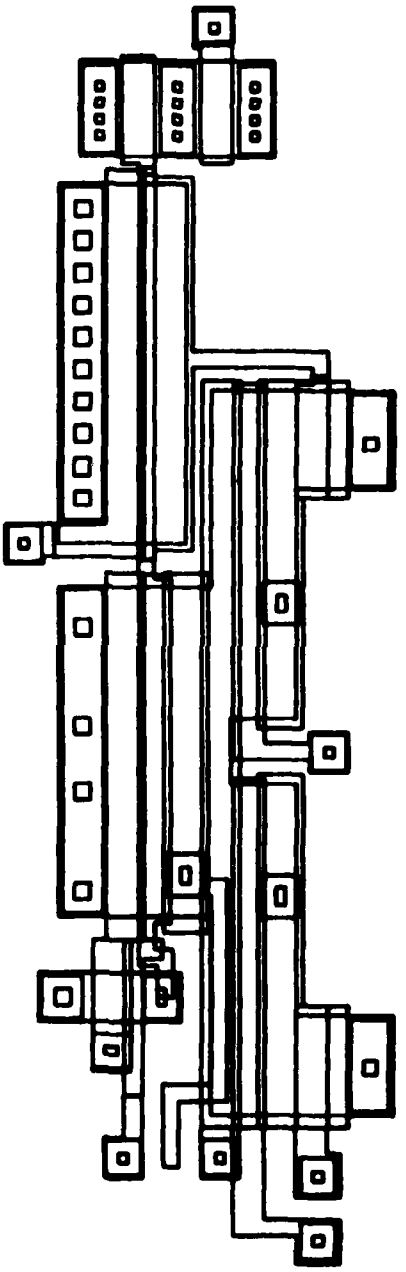


Figure 19. CALMA Layout of Improved SCCD-UDM

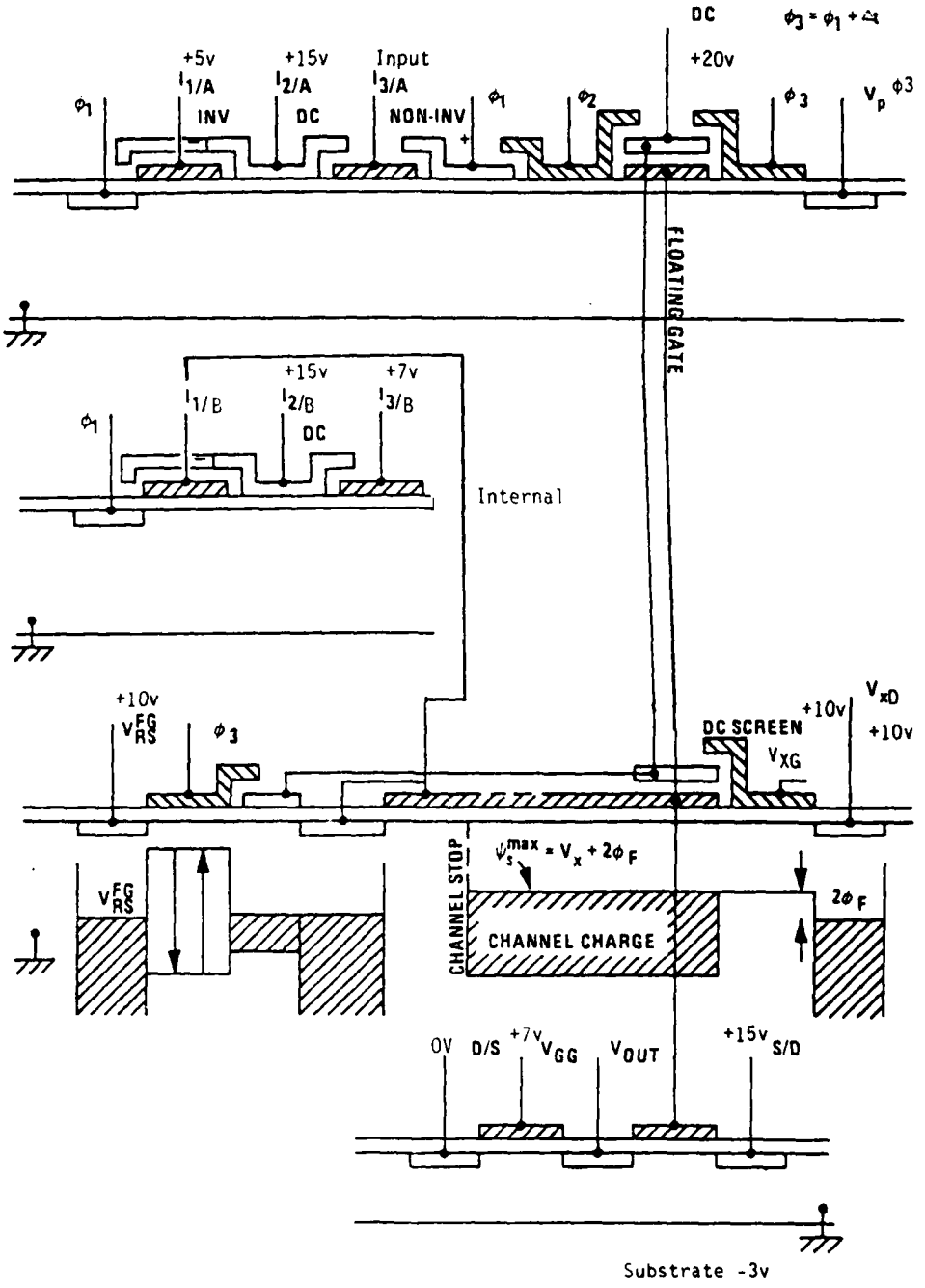


Figure 20. Full Operation

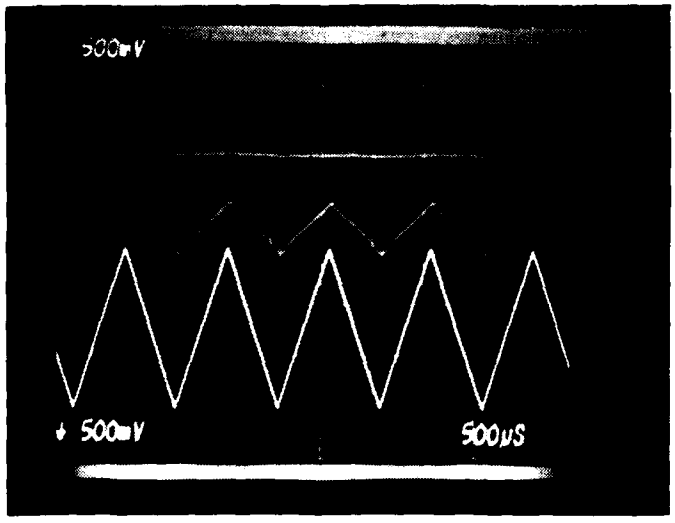


Figure 21. Overall Gain

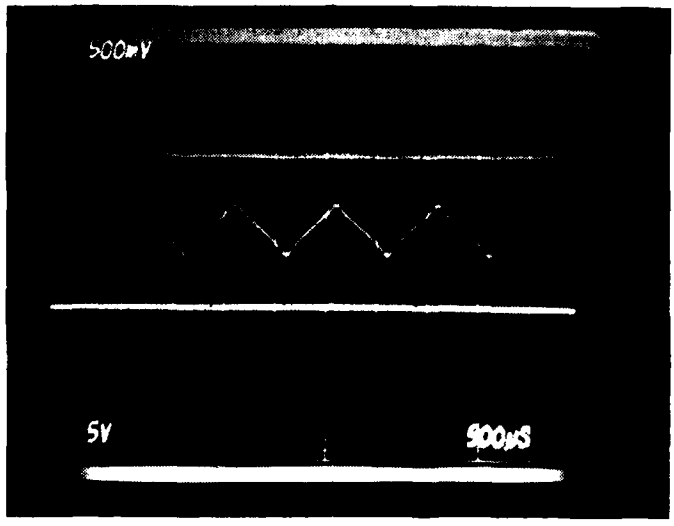
SWITCHED-CAPACITOR UDM TEST STRUCTURES

The initial switched capacitor test structure is illustrated in Figure 23. A photograph of the chip is shown in Figure 24. This simple unit-delay-multiply (UDM) device uses a voltage follower as an output buffer.

The SC has the major advantages of being large signal and infinitely extendable with extra input capacitors C_{1x}. We have designed a single-input capacitor structure with current mirror ratios

$$K_1 = 1/2,\ K_2 = 1,$$

so that a direct measurement of the offsets can be made easily. The values of K are mask programmed by designing the current mirror with duplicate



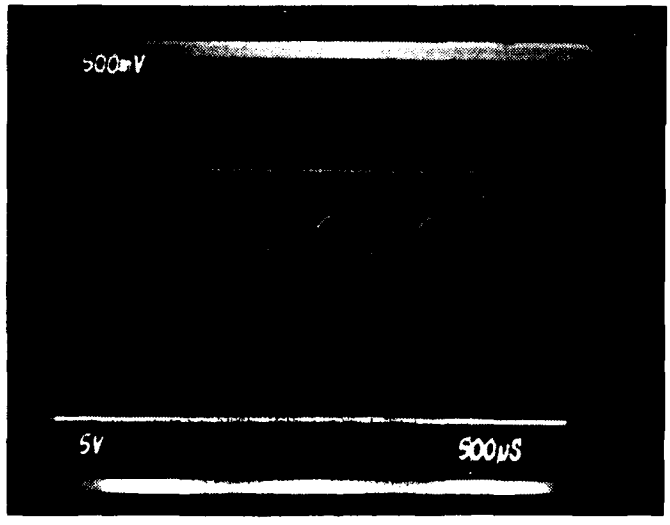


Figure 22. Variation with V_X Gain Control

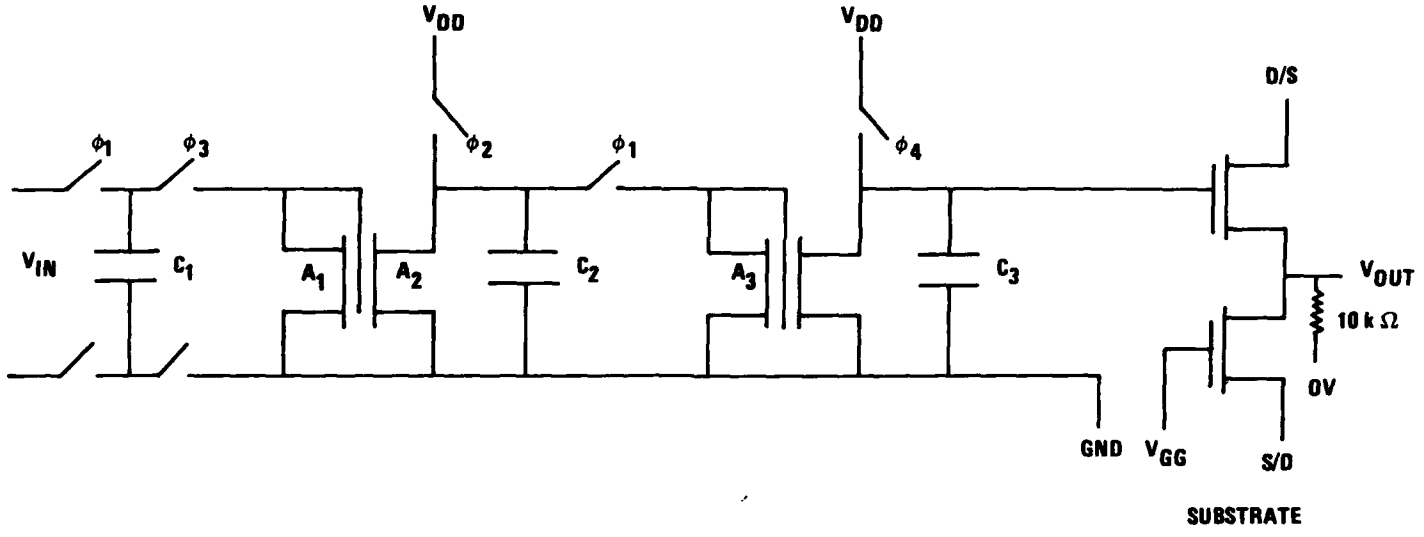


Figure 23. S-C UDM Test Structure Circuit Diagram

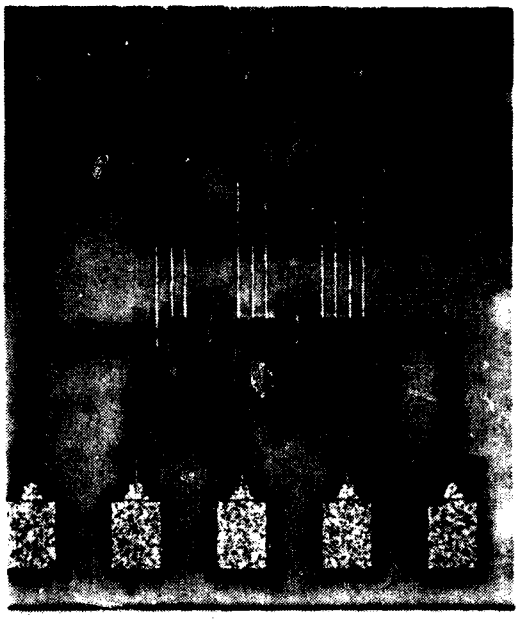


Figure 24. S-C Test Structure

transistor pairs. Connecting two on the input side and one on the output, for example, gives the "half." Since fabrication tolerances should be identical, an accurate measurement of mirror tracking should be possible as a function of frequency. The capacitors are designed to be identical, and are implemented by Poly I and Poly II capacitors with "zero" overlap. The capacitance values, of course, depend on the oxide thickness and on the absolute area, but, to first order, differences should be negligible. Parasitic loading due to the transistor drain/source junctions will limit the linearity of the transfer function, since they are "square law" with voltage. It should be possible to measure the distortion due to that effect on the present structure. Signal lines are screened throughout by using a Poly II shield between Poly I gate and first-level metal.

In Figure 24 above, C_1 is on the left. The structure is arranged to butt at left/right for higher-order sections. As can be seen, the section is very compact with the small capacitors used. The ideal transfer function of a first-order section is shown in Figure 25 for three values of α_1. The phase response is not quite linear, but since the multipliers must sum to unity, the section is unconditionally stable.

During evaluation, the devices were clocked (ϕ_1, ϕ_2, ϕ_3, and ϕ_4) using identical 0-13V nonoverlapping pulses with width $\frac{1}{4f_{clock}}$. Exact details of other test conditions are given in the second interim report.

Linearity in the device is good over a very wide range of input signal frequencies. Nevertheless, we attempted to determine the lowest acceptable clocking frequency. This was done by measuring the longest storage time of the output capacitor in the S-C UDM device.

We varied the ϕ_4 clocking frequency upward from 1 Hz until we found a storage time (= ϕ_4 OFF) for which 90 percent of the initial (ϕ_4 ON) output remained. The results are given in Figure 26, where ϕ_4 (top trace) and V_{OUT} (bottom trace) are shown on an oscillogram. To more easily visualize the percentage reduction of the output signal, the output volts/division were adjusted so that when ϕ_4 was on, the V_{OUT} due to V_{DD} (0 percent droop) was 20 increments above GND (100 percent droop). The time/division was so large that a single-sweep exposure was used. The results indicate a 30 msec storage time will give a reduction of the output signal amplitude of approximately 10 percent. Since the storage time is 30 msec = 3 $T_{clock}/4$, the slowest $f_{clock} = 1/T_{clock} = (40 \text{ msec})^{-1} = 25$ Hz. This time was improved on a subsequent test chip by increasing the value of C_3 and minimizing the mirror diode area.

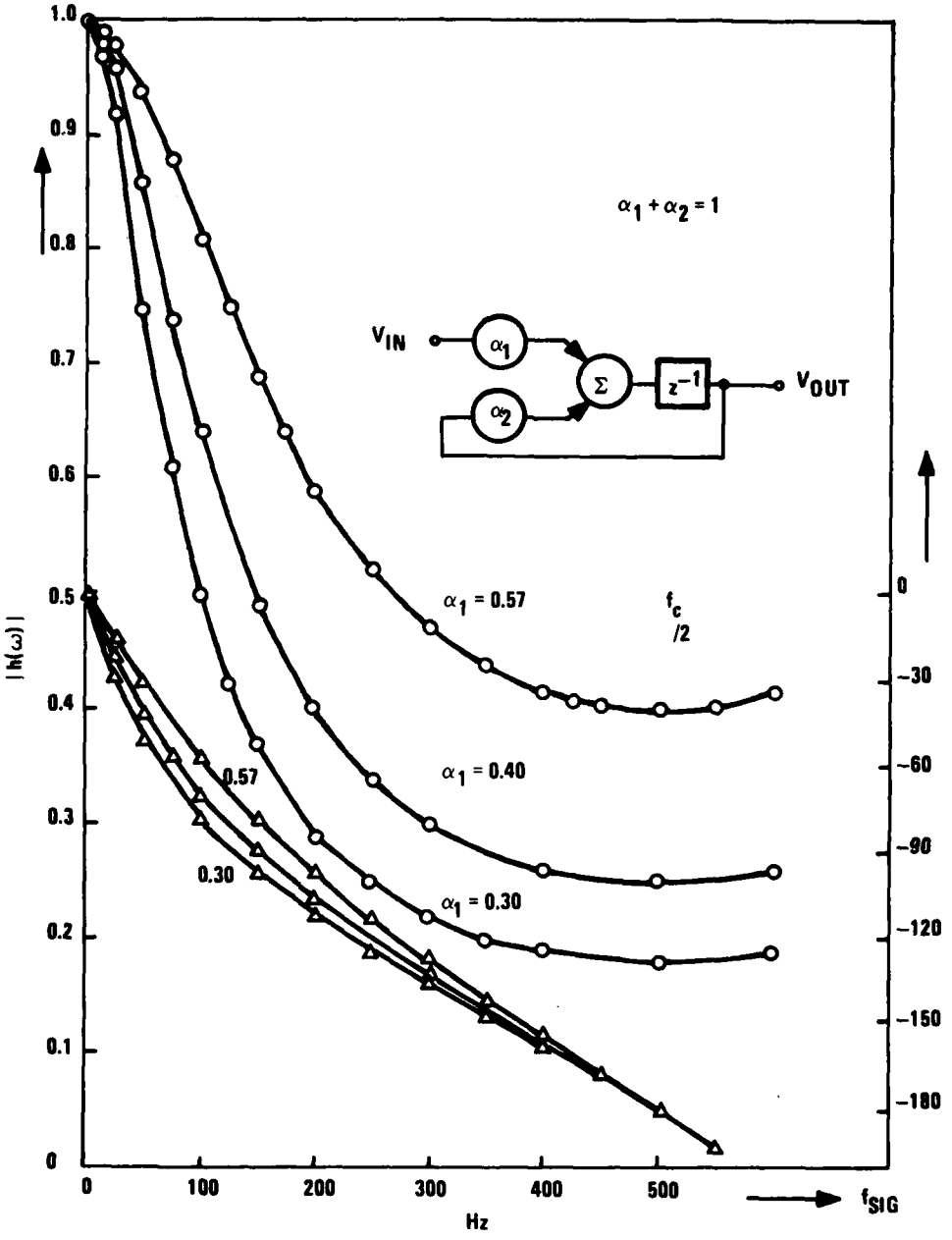
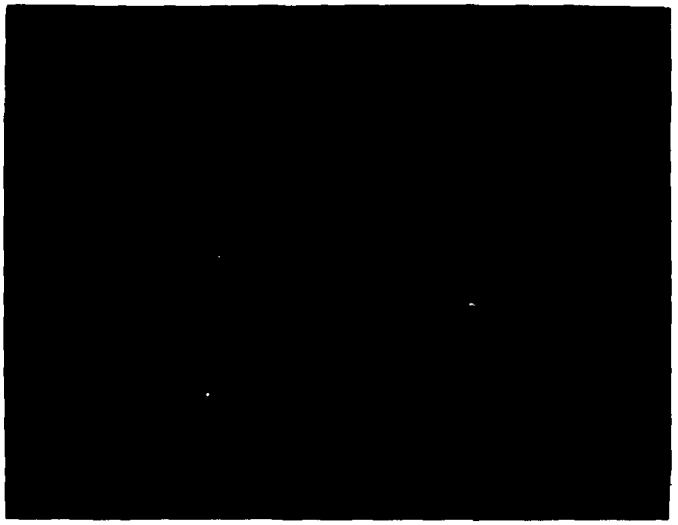


Figure 25. First-Order Recursive Low-Pass Filter



ϕ_4 Top trace

V_{OUT} Lower trace

Figure 26. Storage Time Determination

We then evaluated the high-frequency performance of the current-mirror half section. The maximum clock rate of the section is a parameter of great interest since the section is capable of satisfying many virtual-ground analog circuit functions. For example, transversal filters demonstrated to date have suffered from slew-rate limitation of the on-chip MOS op-amps used for current sensing implementations (that is, PTOF). The slew rate is chiefly determined by the bias current available at the differential input stage and the capacitance at the input node to the differential-to-single-ended converter. In order to maintain stability of the op-amp, a negative feedback capacitor is usually introduced with a value in excess of $\approx$ 10 pF. The op-amp is consequently inherently slower than open-loop MOS buffers.

The current-mirror, however, should be capable of operation at a significantly higher bandwidth than an equivalent op-amp. We verified this assertion using the ISPICE circuit simulator. The current-mirror half-section was modelled using a first-order mobility-field equation. Although not designed for clock rates above a few MHz, the simulations indicated that the voltage transfer function of the half-section is apparently maintained up to 20 MHz.

Figure 27 shows a diagram of the simulated circuit with the nodes, capacitors, and MOSFETs marked. This is followed by Figure 28, a direct copy of the ISPICE printout showing the parameters used in modeling the MOSFETs. Figure 29 is the ISPICE plot of the clocking waveforms and output voltage at C_2 (that is, V(2)) for the 20 MHz transient analysis simulation with V_{IN} = +5V DC. The time scale runs from 0 to 150 nsec with points every 2 nsec.

Next we performed a current tracking experiment that indicated good tracking ability down to the near-nanoampere range.

The current mirror portion (see Figure 30) of our SC-UDM operates on the principle that a charge on C_L produces a gate voltage which turns on both MOSFETs of the current mirror, allowing equal (though not constant) currents I_L and I_R to remove charges Q_L and Q_R from C_L and C_R in a time τ, at which time the voltage remaining across C_L is too small to keep the transistors turned on. Since the MOSFETs are very close together (they share drains), all terms in the equation for the source-to-drain current should be identical for the two transistors, except that we may choose the size of the gates at the design stage which affects the β factors. We then have $Q_L = K_1 Q_R$, and thus $I_L = K_1 I_R$ where, to first order, K_1 is a function of only the geometry of the mirror, so that K_1 should remain constant over any range of Q and I.

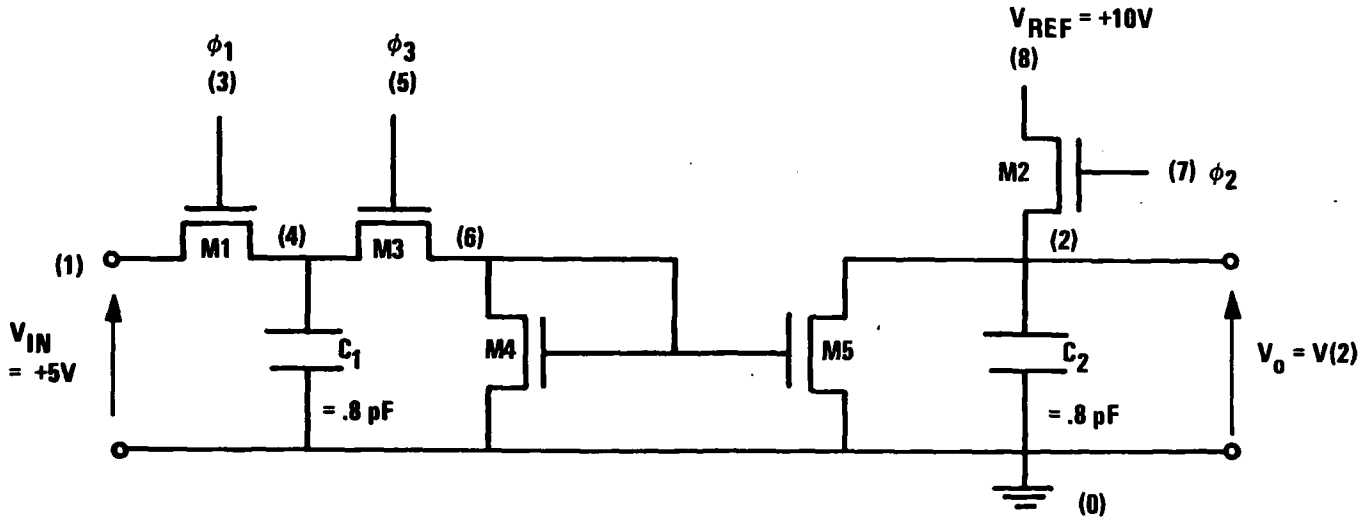


Figure 27. Simulated Switched-Capacitor Current-Mirror Circuit

```
**** MOSFETS

NAME            D       G       S       B       MODEL

M1              1       3       4       0       NMOD
WIDTH = 1.200D-03  LENGTH= 7.000D-04
BAD   = *NOT SET*  SAD   = *NOT SET*  BAS   = *NOT SET*  SAS   = *NOT SET*
TYPE  = NMOS2      VTO   = 1.620D+00  PHI   = 6.150D-01  UO    = 6.000D+02
NB    = 4.125D+15  RD    = 1.000D-01  RS    = 1.000D-01  CO    = 3.140D-08
C1    = 1.570D-12  C2    = 1.570D-12  CBD   = 1.850D-16  CBS   = 1.850D-16
PB    = 8.970D-01  IS    = 1.000D-14  KN    = 0.0        NN    = 0.0
KL    = 0.0        ECRIT = 0.0        BETA  = 9.420D-06  GAMMA = 4.700D-01
LAMBDA=-5.601D-05  KF    = 0.0        AF    = 1.000D+00

M2              8       7       2       0       NMOD
WIDTH = 1.200D-03  LENGTH= 7.000D-04
BAD   = *NOT SET*  SAD   = *NOT SET*  BAS   = *NOT SET*  SAS   = *NOT SET*
TYPE  = NMOS2      VTO   = 1.620D+00  PHI   = 6.150D-01  UO    = 6.000D+02
NB    = 4.125D+15  RD    = 1.000D-01  RS    = 1.000D-01  CO    = 3.140D-08
C1    = 1.570D-12  C2    = 1.570D-12  CBD   = 1.850D-16  CBS   = 1.850D-16
PB    = 8.970D-01  IS    = 1.000D-14  KN    = 0.0        NN    = 0.0
KL    = 0.0        ECRIT = 0.0        BETA  = 9.420D-06  GAMMA = 4.700D-01
LAMBDA=-5.601D-05  KF    = 0.0        AF    = 1.000D+00

M3              4       5       6       0       NMOD
WIDTH = 1.200D-03  LENGTH= 7.000D-04
BAD   = *NOT SET*  SAD   = *NOT SET*  BAS   = *NOT SET*  SAS   = *NOT SET*
TYPE  = NMOS2      VTO   = 1.620D+00  PHI   = 6.150D-01  UO    = 6.000D+02
NB    = 4.125D+15  RD    = 1.000D-01  RS    = 1.000D-01  CO    = 3.140D-08
C1    = 1.570D-12  C2    = 1.570D-12  CBD   = 1.850D-16  CBS   = 1.850D-16
PB    = 8.970D-01  IS    = 1.000D-14  KN    = 0.0        NN    = 0.0
KL    = 0.0        ECRIT = 0.0        BETA  = 9.420D-06  GAMMA = 4.700D-01
LAMBDA=-5.601D-05  KF    = 0.0        AF    = 1.000D+00

M4              6       6       0       0       NMOD
WIDTH = 5.800D-03  LENGTH= 7.000D-04
BAD   = *NOT SET*  SAD   = *NOT SET*  BAS   = *NOT SET*  SAS   = *NOT SET*
TYPE  = NMOS2      VTO   = 1.620D+00  PHI   = 6.150D-01  UO    = 6.000D+02
NB    = 4.125D+15  RD    = 1.000D-01  RS    = 1.000D-01  CO    = 3.140D-08
C1    = 1.570D-12  C2    = 1.570D-12  CBD   = 1.850D-16  CBS   = 1.850D-16
PB    = 8.970D-01  IS    = 1.000D-14  KN    = 0.0        NN    = 0.0
KL    = 0.0        ECRIT = 0.0        BETA  = 9.420D-06  GAMMA = 4.700D-01
LAMBDA=-5.601D-05  KF    = 0.0        AF    = 1.000D+00

M5              2       6       0       0       NMOD
WIDTH = 2.900D-03  LENGTH= 7.000D-04
BAD   = *NOT SET*  SAD   = *NOT SET*  BAS   = *NOT SET*  SAS   = *NOT SET*
TYPE  = NMOS2      VTO   = 1.620D+00  PHI   = 6.150D-01  UO    = 6.000D+02
NB    = 4.125D+15  RD    = 1.000D-01  RS    = 1.000D-01  CO    = 3.140D-08
C1    = 1.570D-12  C2    = 1.570D-12  CBD   = 1.850D-16  CBS   = 1.850D-16
PB    = 8.970D-01  IS    = 1.000D-14  KN    = 0.0        NN    = 0.0
KL    = 0.0        ECRIT = 0.0        BETA  = 9.420D-06  GAMMA = 4.700D-01
LAMBDA=-5.601D-05  KF    = 0.0        AF    = 1.000D+00


ISPICE: >probe op m1 m2 m3 m4 m5

**** MOSFETS

NAME          MODEL          VGS       VDS       VBS       ID

M1            NMOD          -2.610     2.390    -2.610   -2.651D-05
M2            NMOD          -8.102     1.898    -8.102   -5.847D-05
M3            NMOD          -1.672     0.938    -1.672   -8.211D-05
M4            NMOD           1.672     1.672     0.0      1.392D-07
M5            NMOD           1.672     8.102     0.0     -1.295D-05
```

Figure 28. Parameters Used for ISPICE Simulation

```
ISPICE 2.09   (19SEP80) - 19JAN81 17:03:45

TRAN SIMULATION OF CIRCUIT: SC

LEGEND
*  : TIME
+1 : V(3)
+2 : V(7)
+3 : V(5)
+4 : V(2)
```

X	Y1	Y2	Y3	Y4	0.0 5.000E+00 1.000E+01 1.500E+01
0.0	0.0	0.0	0.0	0.0	*
2.000E-09	7.500E+00	0.0	0.0	0.0	*
4.000E-09	1.500E+01	0.0	0.0	0.0	*
6.000E-09	1.500E+01	0.0	0.0	0.0	*
8.000E-09	1.500E+01	0.0	0.0	0.0	*
1.000E-08	1.500E+01	0.0	0.0	0.0	*
1.200E-08	1.500E+01	0.0	0.0	0.0	*
1.400E-08	7.500E+00	0.0	0.0	0.0	*
1.600E-08	0.0	0.0	0.0	0.0	*
1.800E-08	0.0	0.0	0.0	0.0	*
2.000E-08	0.0	1.500E+01	0.0	1.774E+00	*
2.200E-08	0.0	1.500E+01	0.0	4.706E+00	*
2.400E-08	0.0	1.500E+01	0.0	6.282E+00	*
2.600E-08	0.0	1.500E+01	0.0	7.254E+00	*
2.800E-08	0.0	1.500E+01	0.0	7.905E+00	*
3.000E-08	0.0	1.500E+01	0.0	8.366E+00	*
3.200E-08	0.0	2.746E-14	0.0	8.280E+00	*
3.400E-08	0.0	0.0	0.0	8.280E+00	*
3.600E-08	0.0	0.0	7.500E+00	8.285E+00	*
3.800E-08	0.0	0.0	1.500E+01	8.111E+00	*
4.000E-08	0.0	0.0	1.500E+01	7.863E+00	*
4.200E-08	0.0	0.0	1.500E+01	7.673E+00	*
4.400E-08	0.0	0.0	1.500E+01	7.524E+00	*
4.600E-08	0.0	0.0	1.500E+01	7.406E+00	*
4.800E-08	0.0	0.0	7.500E+00	7.327E+00	*
5.000E-08	0.0	0.0	0.0	7.321E+00	*
5.200E-08	7.500E+00	0.0	0.0	7.321E+00	*
5.400E-08	1.500E+01	0.0	0.0	7.321E+00	*
5.600E-08	1.500E+01	0.0	0.0	7.321E+00	*
5.800E-08	1.500E+01	0.0	0.0	7.321E+00	*
6.000E-08	1.500E+01	0.0	0.0	7.321E+00	*
6.200E-08	1.500E+01	0.0	0.0	7.321E+00	*
6.400E-08	7.500E+00	0.0	0.0	7.321E+00	*
6.600E-08	0.0	0.0	0.0	7.321E+00	*
6.800E-08	0.0	0.0	0.0	7.321E+00	*
7.000E-08	0.0	1.500E+01	0.0	7.544E+00	*
7.200E-08	0.0	1.500E+01	0.0	8.108E+00	*
7.400E-08	0.0	1.500E+01	0.0	8.514E+00	*
7.600E-08	0.0	1.500E+01	0.0	8.815E+00	*
7.800E-08	0.0	1.500E+01	0.0	9.046E+00	*
8.000E-08	0.0	1.500E+01	0.0	9.224E+00	*
8.200E-08	0.0	8.586E-13	0.0	9.132E+00	*
8.400E-08	0.0	0.0	0.0	9.132E+00	*
8.600E-08	0.0	0.0	7.500E+00	9.131E+00	*
8.800E-08	0.0	0.0	1.500E+01	8.863E+00	*
9.000E-08	0.0	0.0	1.500E+01	8.577E+00	*
9.200E-08	0.0	0.0	1.500E+01	8.358E+00	*
9.400E-08	0.0	0.0	1.500E+01	8.189E+00	*
9.600E-08	0.0	0.0	1.500E+01	8.056E+00	*
9.800E-08	0.0	0.0	7.500E+00	7.967E+00	*
1.000E-07	0.0	0.0	0.0	7.961E+00	*
1.020E-07	7.500E+00	0.0	0.0	7.960E+00	*
1.040E-07	1.500E+01	0.0	0.0	7.960E+00	*
1.060E-07	1.500E+01	0.0	0.0	7.960E+00	*
1.080E-07	1.500E+01	0.0	0.0	7.960E+00	*
1.100E-07	1.500E+01	0.0	0.0	7.959E+00	*
1.120E-07	1.500E+01	0.0	0.0	7.959E+00	*
1.140E-07	7.500E+00	0.0	0.0	7.959E+00	*
1.160E-07	0.0	0.0	0.0	7.959E+00	*
1.180E-07	0.0	0.0	0.0	7.959E+00	*
1.200E-07	0.0	1.500E+01	0.0	8.136E+00	*
1.220E-07	0.0	1.500E+01	0.0	8.534E+00	*
1.240E-07	0.0	1.500E+01	0.0	8.831E+00	*
1.260E-07	0.0	1.500E+01	0.0	9.057E+00	*
1.280E-07	0.0	1.500E+01	0.0	9.234E+00	*
1.300E-07	0.0	1.500E+01	0.0	9.373E+00	*
1.320E-07	0.0	2.428E-12	0.0	9.278E+00	*
1.340E-07	0.0	0.0	0.0	9.277E+00	*
1.360E-07	0.0	0.0	7.500E+00	9.277E+00	*
1.380E-07	0.0	0.0	1.500E+01	9.007E+00	*
1.400E-07	0.0	0.0	1.500E+01	8.720E+00	*
1.420E-07	0.0	0.0	1.500E+01	8.501E+00	*
1.440E-07	0.0	0.0	1.500E+01	8.331E+00	*
1.460E-07	0.0	0.0	1.500E+01	8.198E+00	*
1.480E-07	0.0	0.0	7.500E+00	8.109E+00	*
1.500E-07	0.0	0.0	0.0	8.102E+00	*

```
ISPICE:
```

Figure 29. ISPICE Simulation Output: Circuit Output Voltage and Clocking Waveforms

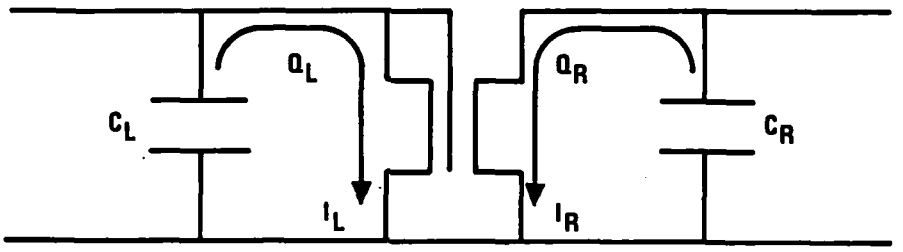


Figure 30. Current Mirror Portion of SC-UDM

Rather than charging and discharging the capacitors and measuring two different charges, we used a current source to vary the input current (I_L) over six orders of magnitude and then measured the resulting output current. It should be noticed that turning ϕ_1 on to access the first current mirror also turns on the second current mirror so a measurement of I_{DD} includes current through both T_2 and T_3. However, the area of the first MOSFET gate A_1 is designed to be equal to the sum of the areas of the other two gates, A_2 and A_3. Thus the ratio of currents should be unity. We may still test our linearity assumption using this type of setup. Figure 31 shows that the current tracking ability of the mirror is quite good down to the near-nanoampere range where sub-V_T current flow dominates. Although this low current non-tracking is not a problem with filter circuitry, it is the limiting characteristic for A/D applications. Surface state annealing treatments can be incorporated in the fabrication process to minimize this effect. This was not done for the present samples. To confirm that this was the mechanism limiting linearity/tracking, the input and output I-V characteristics were plotted to show the sub-V_T regime. The change-over point at extrapolated V_T is indicated in Figure 31.

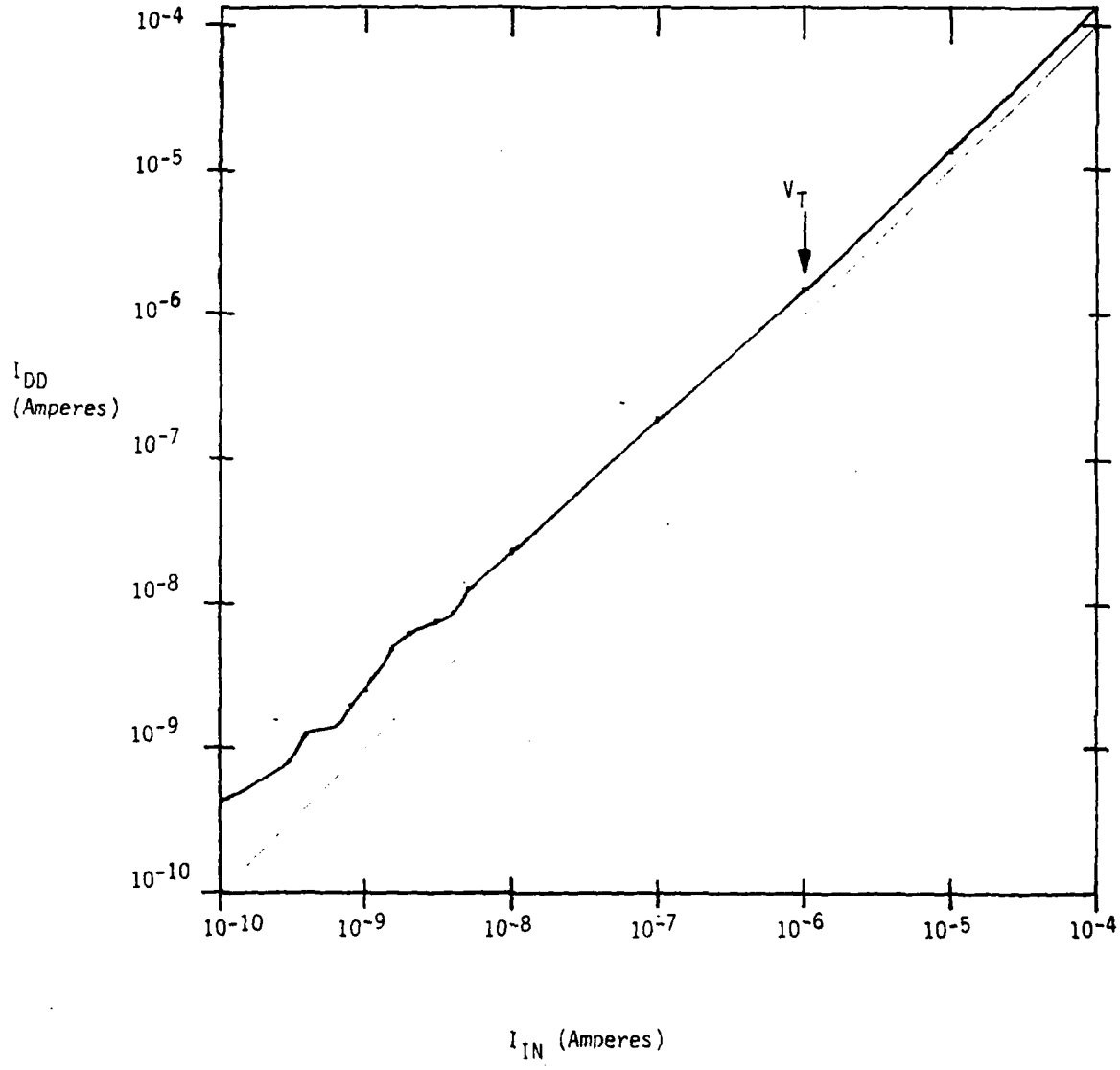


Figure 31. Results of Current Tracking Experiment

The switched-capacitor UDM structure was then modified to yield a first-order, low-pass recursive SC filter. A feedback line was added from the output capacitor to the input current mirror, as shown in Figure 32. Calma layout of this device is shown in Figure 33.

When the new circuit was evaluated by attempting to drive the output buffer via V_{DD}/ϕ_4, the output voltage was zero, indicating a possible short circuit to ground in the general vicinity of the ϕ_4 switch. This assumption is reinforced by the fact that a 0.6mA current can be observed in the V_{DD} line (ϕ_2 OFF) when ϕ_4 is turned on. We are able to drive the output buffer by applying a $+V_{IN}$, closing only ϕ_1 and ϕ_3 and leaving the $-V_{IN}$ terminal open circuit. A 2.0v input swing gives a 0.4v output voltage swing, indicating an output buffer gain of 0.2. No further analysis of this circuit is planned for during the remainder of the contract period. Despite the failure of this test circuit, the circuit concept is credible, and we believe that had the device been operative, it would indeed have shown a low pass filter characteristic.

NMOS OPERATIONAL AMPLIFIER TEST CIRCUIT

Proper evaluation of the current mirror approach to scaling (which can eliminate the need for operational amplifiers in conjunction with switched-capacitor circuitry) required fabrication of an NMOS op amp test circuit for comparison.

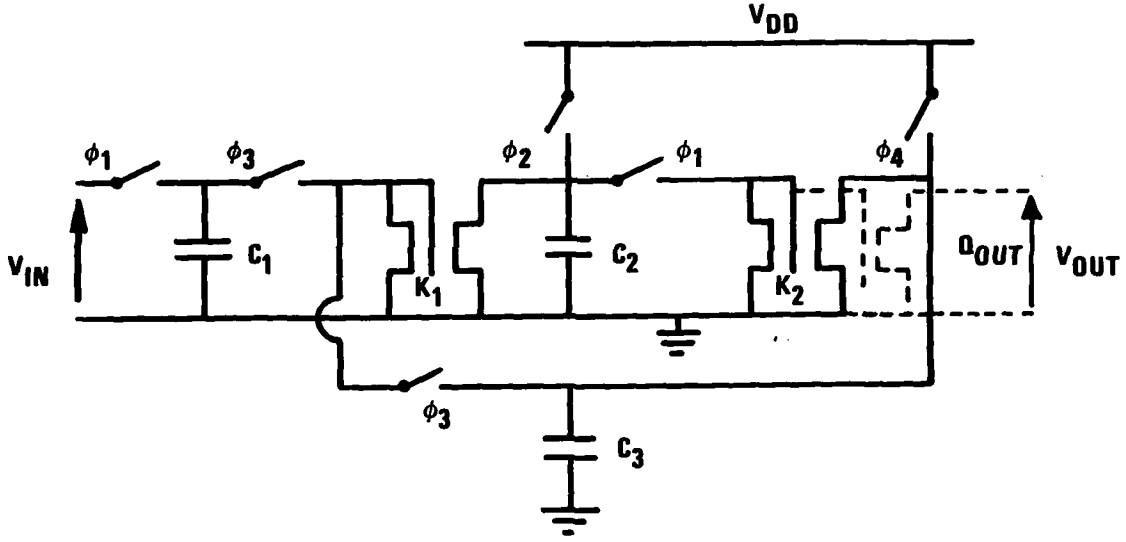


Figure 32. Recursive Low-Pass Filter

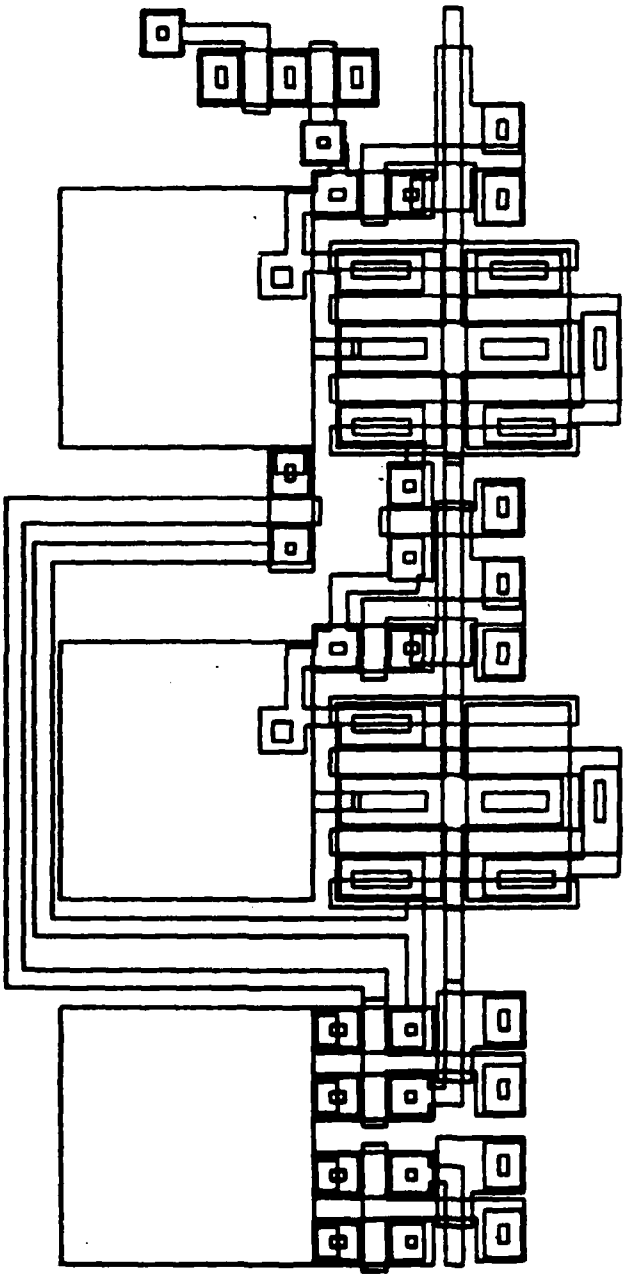


Figure 33. CALMA Layout of First-Order Low-Pass Recursive SC Filter

The operational amplifier[3] schematic is Figure 34. For all of our tests, we kept three terminals at constant voltages: V_{DD} = +20v, substrate = 0v (GND), and GND = 0v. The +20v V_{DD} was chosen because it appeared to give the best voltage swing for various inputs. Input offsets are extremely high for both the common-mode and differential-mode gains. The other two inputs, +IN and -IN, were either +5v D.C. or a 1v peak-to-peak sine wave (offset = +5v).

The first two oscillograms of Figure 35 show the A.C. inputs and the A.C. output measured at the left side of the 6pF capacitor. The gain is about 2.75. The third oscillogram shows V_{+IN} with respect to V_{OUT}; notice that the gain (2.5) is lower, indicating a fractional gain factor between the LHS of the capacitor and V_{OUT}. This is a serious limitation in the operation of the device as an operational amplifier. Figure 36 is a spectrum analyzer oscillogram showing that this fractional gain characteristic appears over a large frequency range. A D.C. gain, $\frac{\Delta V_{OUT}}{\Delta V_{-IN}}$, of 2 was also observed.

A test to determine the input offset voltage, and another involving a feedback resistor to the -IN terminal were attempted, but no conclusive results were obtained.

The operational amplifier was not fabricated with the transistor dimensions tabulated in the reference paper. However, the aspect ratios (w/ℓ) were not changed, so no explanation is offered for the low gain.

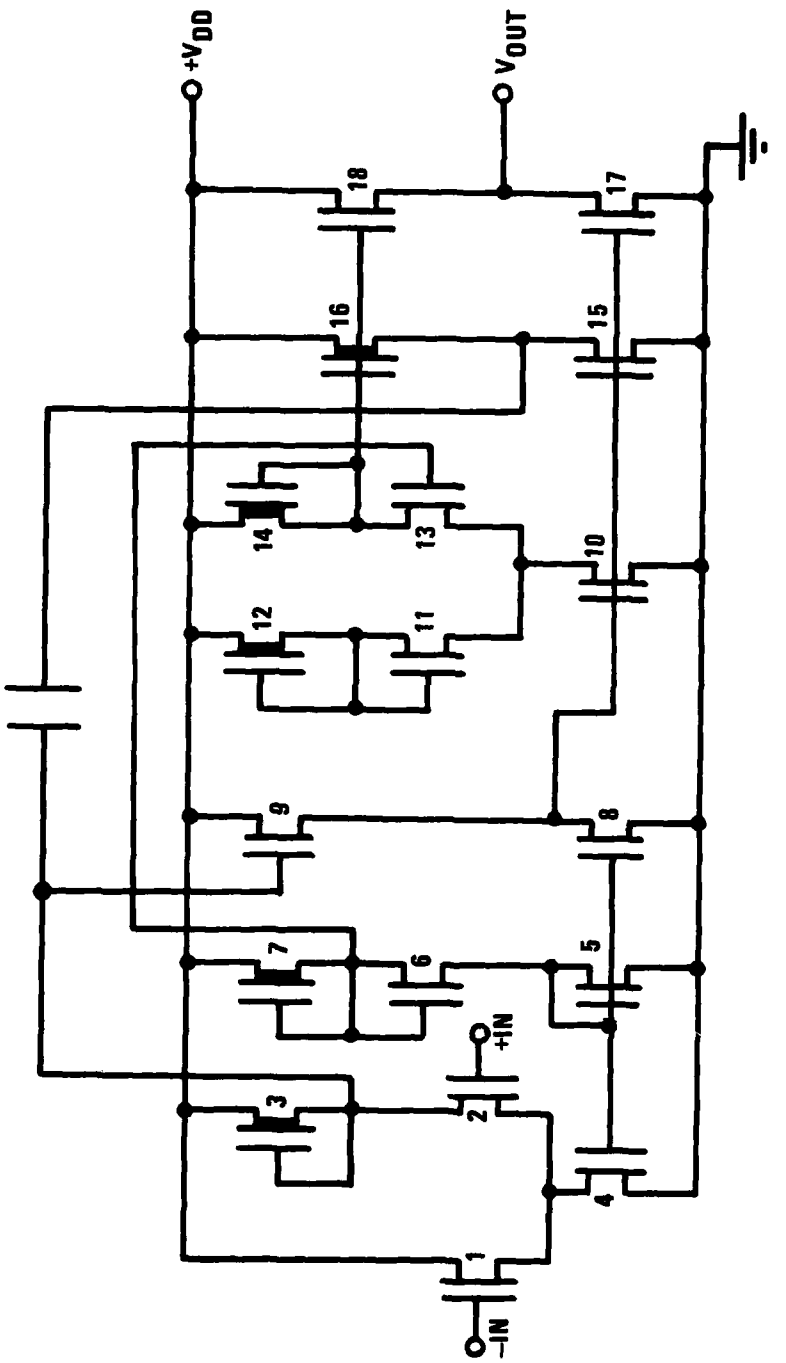


Figure 34. NMOS Operational Amplifier

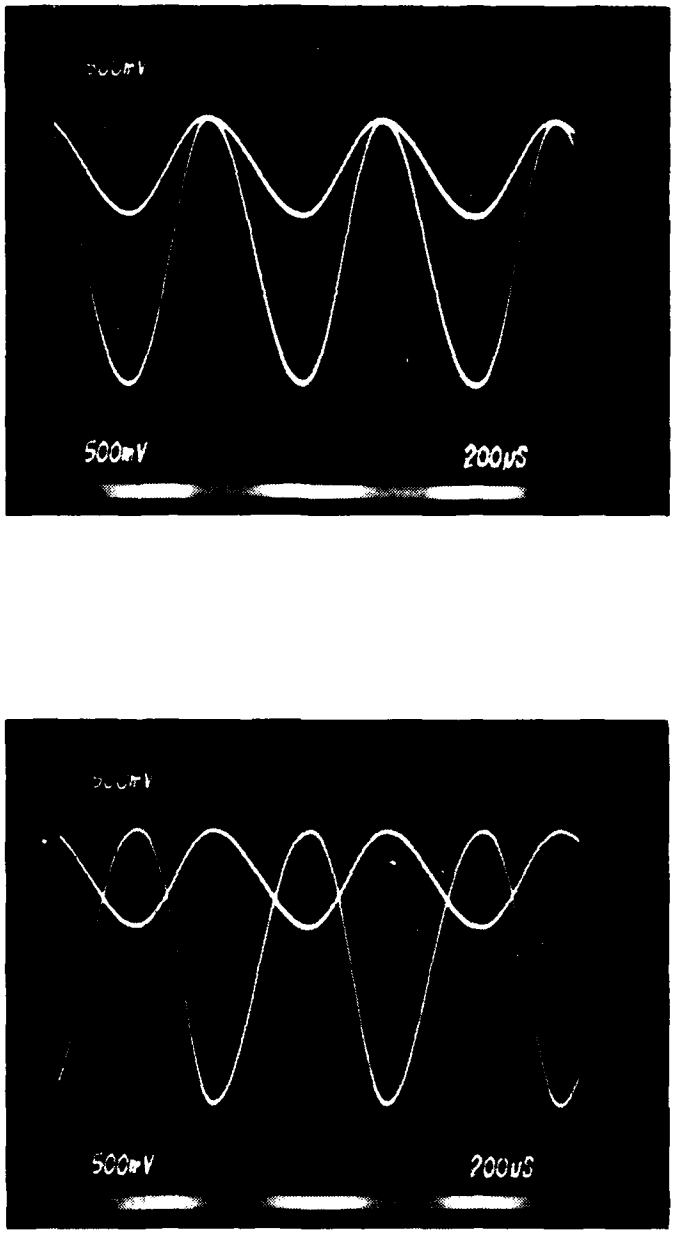


Figure 35. A.C. Gain Difference For NMOS OP Amp

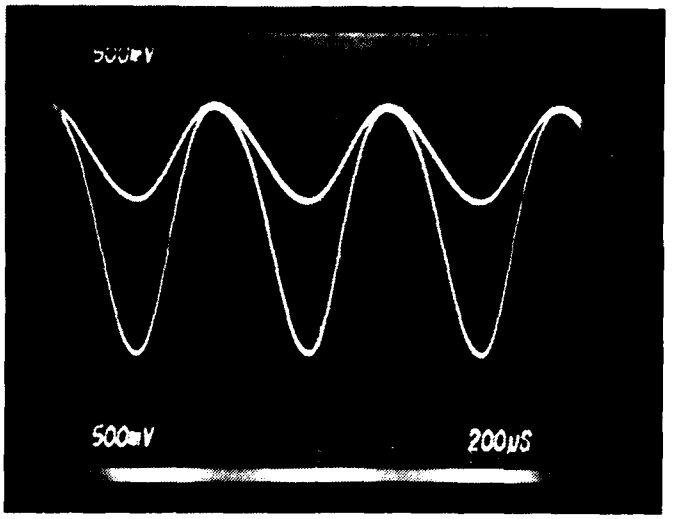


Figure 35. A.C. Gain Difference For NMOS OP Amp (concluded)

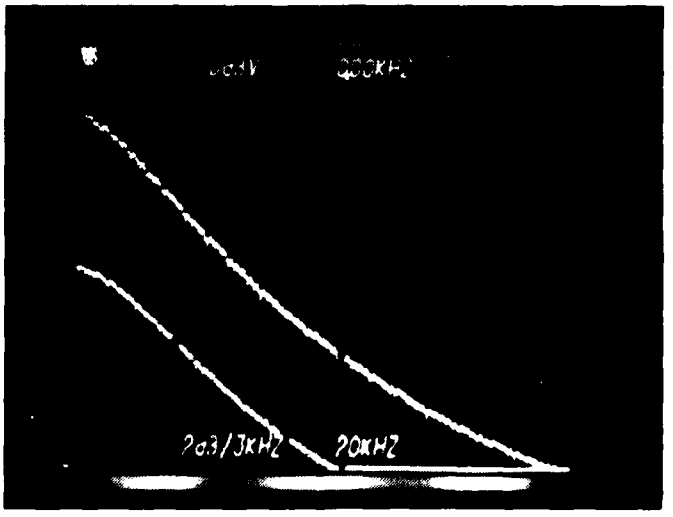


Figure 36. A.C. Gain Difference Via Spectrum Analyser

CURRENT SPLITTER TEST CIRCUIT

A current splitter test structure was also designed and fabricated. Such a circuit is used for high-precision, input-current scaling.

A simplified circuit is shown in Figure 37. The positive input current flows into parallel capacitances $C_1 + C_2$ when switches T_1 and T_3 are open and T_2 is closed. Charging time is limited to keep the required value of capacitance to a minimum at 10V max. We obtain a scale factor of 1/100 or 1/400 if we put $C_1 = 99C_2$ or $C_1 = 399C_2$, for example. The limit to precision is determined by the accuracy to which C_1 does not, in fact, equal $(n - 1)\, C_2$.

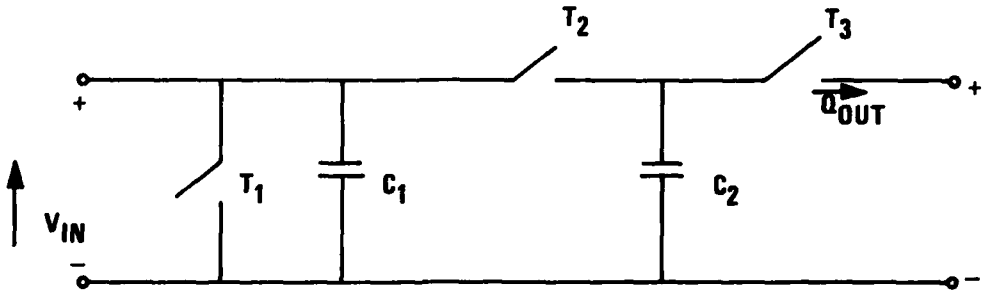


Figure 37. Current Splitter

The center band of Figure 38 shows the high-precision charge divider, one capacitor of which is made up of a block of 23 identical capacitor cells connected in parallel. This gives an input/output capacitance ratio, N, of 23. The switching portion of the circuit is shown more clearly in Figure 39. The capacitor cell, which was chosen to be hexagonal in order to

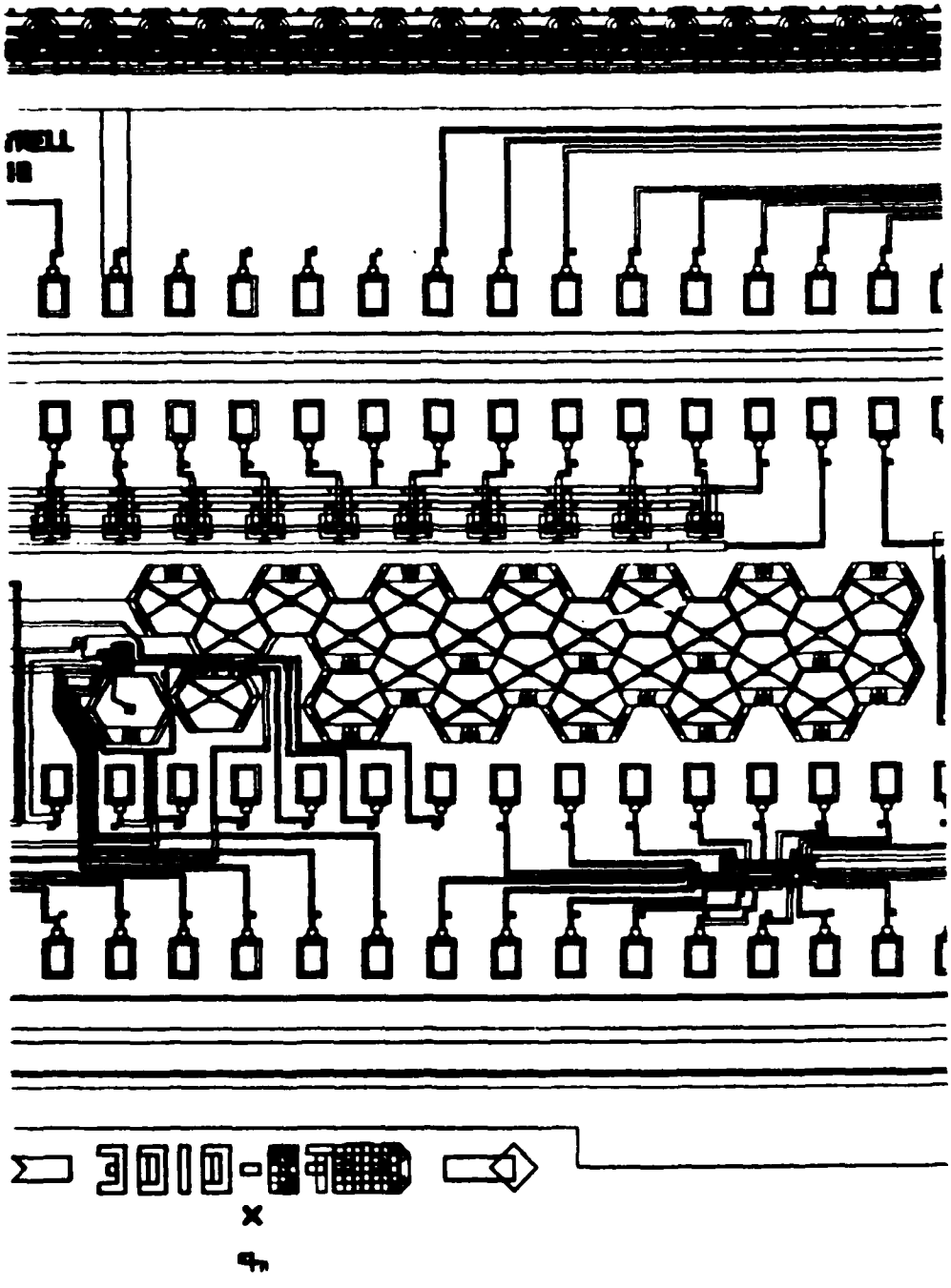


Figure 38. CALMA Layout of Charge Divider

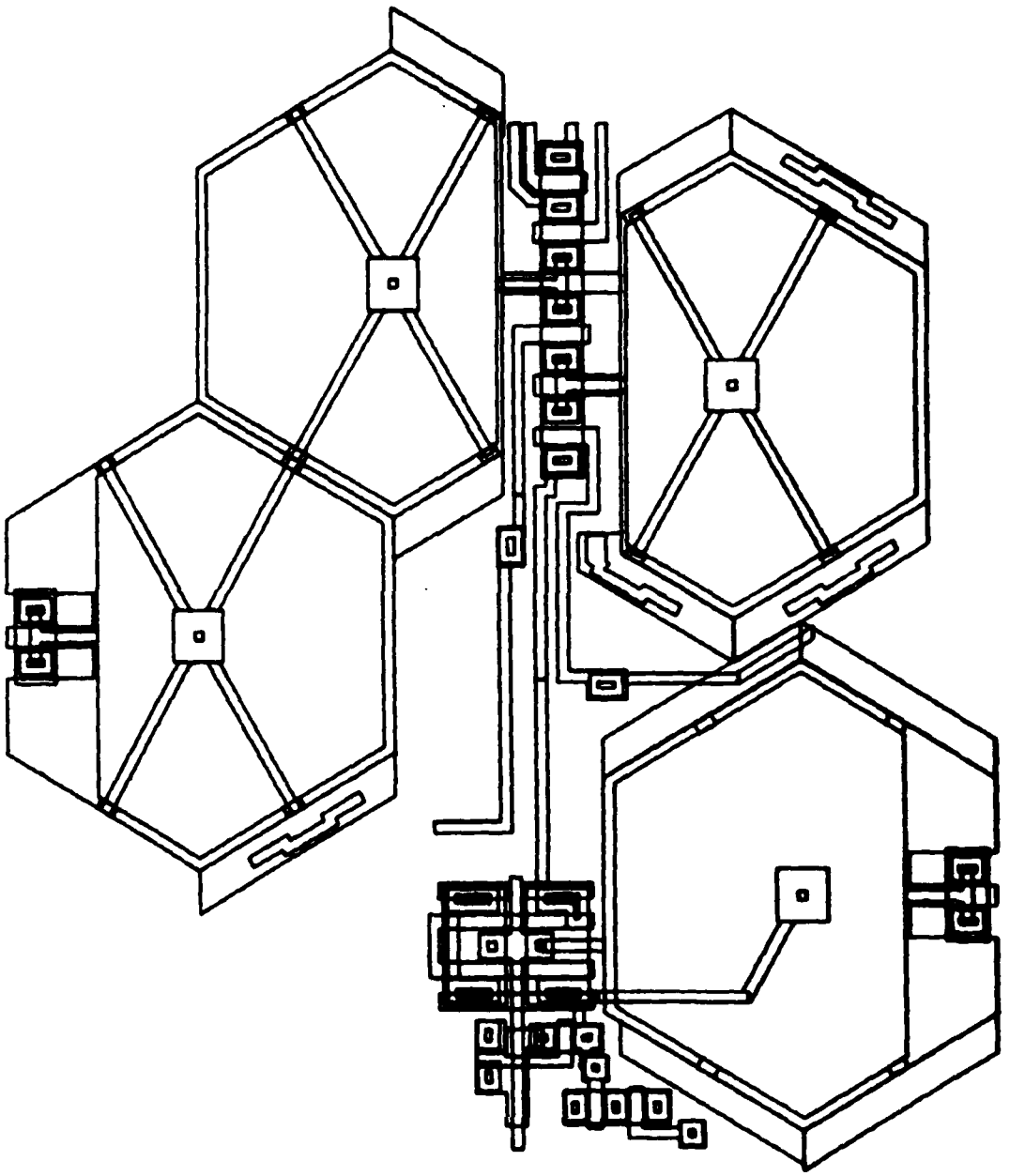


Figure 39. CALMA Layout of Switching Portion of Charge Divider

maximize the packing density, is illustrated in Figure 40. The gate structure on the right side is functional on only two of the cells, but was used repeatedly to make all cells identical and thus improve the capacitor ratio accuracy. This test circuit will enable us to determine the precision with which our process can be used to fabricate capacitance ratios.

Evaluation of this test structure was incomplete at the time of the final report.

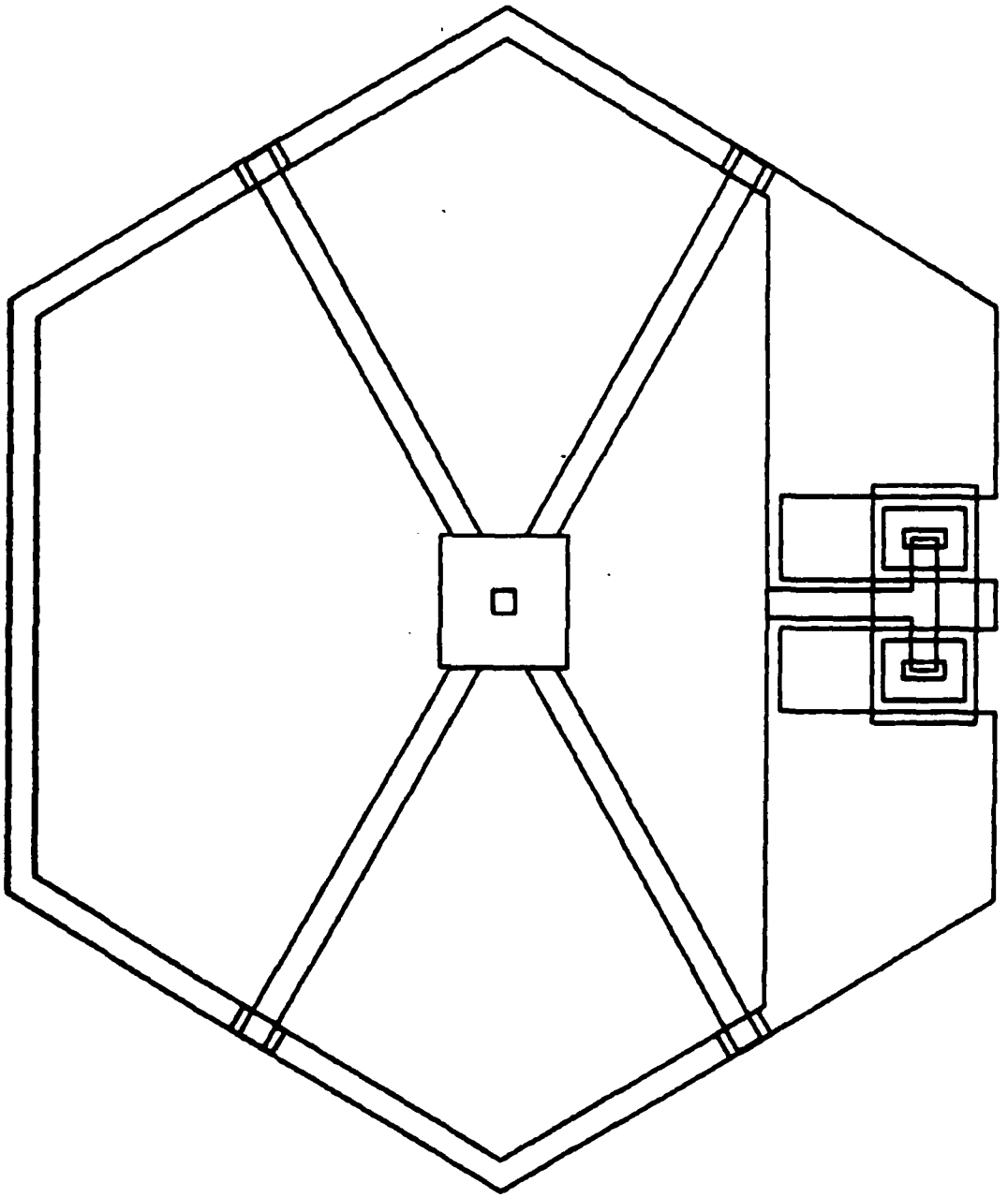


Figure 40. CALMA Layout of Capacitor Cell

SECTION 5

CONCLUSIONS AND RECOMMENDATIONS

In this section we present a brief summary of the major results of the study and the additional work, if any, needed to support each conclusion.

In CCD modeling, we extended earlier modeling results to include more detailed analysis of filter distortion effects resulting from voltage sensing errors in both surface and buried-channel filter structures. We also analyzed CTI effects on filter distortion. Rather than take the conventional approach to filter predistortion to correct for CTI effects, we recommended optimization of the filter coefficients so that the output response is within specifications over a broad range of ε values. More analysis is needed in this area.

We also extended CCD modeling to include certain types of floating-gate sensing structures useful both in synthesis of recursive filter structures and in development of novel CCD analog processing elements (e.g., Honeywell's matrix processing device).

In CCD evaluation, we demonstrated a novel technique for allowing matrix gain setting on a pixel-by-pixel basis rather than globally. This might be done in Honeywell's matrix processor, for example, by using a floating-gate sensor.

In switched-capacitor filtering, we have demonstrated a high-performance current mirror structure that can eliminate the need for most or all operational amplifiers. The low-frequency performance is comparable, and the high-frequency performance superior to op amps, although second-order mobility-field relationships should be used for a more detailed simulation of the structure.

Finally, although results on the structure are incomplete, we developed a high-precision, compact, current-splitter circuit that uses a hexagonal capacitor structure to minimize area.

REFERENCES

1. Broderson, R.W., Hewes, C.R., and Buss, D.D., "A 500-Stage CCD Transversal Filter for Spectral Analysis," IEEE Journal on Solid State Circuits, Vol. SC-11, No. 75, 1976.

2. Arreola, J.I., et al., "Simple Implementation of Sampled-Data Filters Using Current Multipliers, Switches, and Capacitors," Electronics Letters, Vol. 15, No. 24, November 22, 1979.

3. B.J. Hosticka, R.W. Brodersen, and P.R. Gray, "MOS Sampled Data Recursive Filters Using Switched Capacitor Integrators," IEEE Journal on Solid-State Circuits, Vol. SC-12, pp. 600-608, December 1977.

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